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INTERIM TECHNICAL REPORT SUBMITTED TO ADVANCED RESEARCH PROJECTS AGENCY ARLINGTON, VIRGINIA 22209

LASER AND ELECTRON BEAM PROCESSING OF SEMICONDUCTORS: CW BEAM-RECRYSTALLIZED POLYSILICON AS A DEVICE-WORTHY MATERIAL

BY
STANFORD UNIVERSITY
STANFORD, CALIFORNIA 94305

FOR THE PERIOD
JANUARY 1, 1978 THROUGH
DECEMBER 31, 1980

MDA 903-78-C-0128
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Dr. James F. Gibbons
Program Manager and Principal Investigator
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LASER AND ELECTRON BEAM PROCESSING OF SEMICONDUCTORS
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Principal Investigator -- J. F. Gibbons

I. INTRODUCTION

Research on the use of directed energy sources, particularly cw lasers and electron beams, for semiconductor processing operations has been carried out at Stanford under the principal sponsorship of DARPA since January 1, 1978. Over the two years from January 1, 1978 to December 31, 1980, research effort has been concentrated on three principal topics:

(1) Use of lasers and electron beams for annealing ion implanted silicon under solid phase conditions;

(2) Use of lasers and arc sources for recrystallization of thin polysilicon films and a study of the device potential of this material; and

(3) Use of cw lasers and electron beams for promoting metal silicide reactions.

In the following report we collect papers that describe the cw beam recrystallization of thin polysilicon films and the use of this material for device and integrated circuit fabrication. A subsequent report will collect and summarize papers on silicide formation.

SUMMARY OF STANFORD PAPERS ON CW BEAM RECRYSTALLIZATION

OF POLYSILICON FILMS WITH DEVICE APPLICATIONS

Research at Stanford on the use of cw lasers for recrystallization of polysilicon films has led to the publication of 18 original papers and more than 20 reviews. The central contributions contained in this work are summarized briefly below with reference to the attached papers:

- Papers 1 and 2 describe the effects of varying the power level in the cw beam recrystallization of LPCVD polycrystalline silicon films, leading to an experimental determination of the mechanism by which large grains ($2\mu x25\mu$) can be caused to grow from continuous films in which the original grain size is 200-500 Å. Preliminary measurements of the resistivity of these beam-recrystallized films are also included in these papers.

- Papers 3 and 4 describe experiments performed to measure the resistivity reduction obtainable in heavily doped polycrystalline films, using both cw and pulsed laser recrystallization techniques, together with a study of the effect of subsequent heat treatment on resistivity changes produced by the laser processing.

- Paper No. 5 describes the crystal structure and thermal oxidation characteristics of laser-recrystallized polycrystalline silicon, providing data which are essential for the application of this material to device fabrication.

- Papers 6 and 7 describe experiments performed to determine the interface properties at both the back surface of a laser-recrystallized polysilicon film on an insulator and at the underlying interface between the insulator and a single crystal silicon substrate. These measurements show that interface charge densities can be low enough to permit fabrication of high quality devices.

- Papers 8 through 12 describe the fabrication of thin film MOSFETs and MESFETs on the top surface of a laser annealed polycrystalline silicon film. In all cases the results are comparable to those obtained when similar devices are fabricated on single crystal silicon substrates, and in some cases superior to devices fabricated in silicon-on-sapphire substrates.

- Paper 13 describes a one-gate-wide CMOS inverter in which a single gate is used for both n-channel and p-channel devices by using bulk silicon for the p-channel device and an overlying laser-recrystallized silicon film for the n-channel device. This is believed to be the first active device fabricated on separate, vertically-arranged films of material.

- Papers 14 through 16 describe experiments in which a scanning cw laser system is used to fabricate single-crystal <100> silicon islands on amorphous substrates and to promote the lateral epitaxial recrystallization of amorphous silicon films deposited over exposed regions of single crystal silicon substrates.

- Paper 17 gives a review of work on thin film MOSFETs carried out in collaboration with a number of industrial laboratories and includes original material on minority carrier lifetimes and generation rates in laser recrystallized polysilicon films.

- Paper 18 gives a review of the field of thin film MOSFET fabrication prepared as an invited paper for the Laser and Electron Beam Processing Symposium (Material Research Society Meeting, Boston, 1981) and includes original material the velocity-electric field characteristics of the material and the first use of a scanning xenon arc source for recrystallization of polysilicon films.

OVERVIEW OF STANFORD PAPERS ON

CW BEAM-RECRYSTALLIZED POLYSILICON AS A DEVICE-WORTHY MATERIAL

Paper No. 1.

"CW Laser Anneal of Polycrystalline Silicon: Crystalline Structure, Electrical Properties", A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng, and J. D. Hong, Applied Physics Letters 33, 8, (Oct. 15, 1978).

0.4-μm-thick polycrystalline silicon deposited in a low-pressure CVD reactor was implanted with B to a dose of $5 \times 10^{14}/cm^2$ and then irradiated in a cw laser scanning apparatus. The laser annealing produced an increase in grain size from ~ 500 A to long narrow crystals of the order of ~ 25x2 μ, as observed by TEM. Each grain was found to be defect free and extended all the way to the underlying Si_3N_4. Electrical measurements show 100% doping activity with a Hall mobility of about 45 cm^2/V sec, which is close to single-crystal mobility at the same carrier concentration. Thermal annealing produces material with an average gain size of 1000 A and a resistivity higher by a factor of 2.2 than that obtained with the laser anneal. Laser annealing performed after a thermal anneal reduces the resistivity to approximately the same value obtained by laser annealing only.

Paper No. 2.

"Effect of Power Level in CW Laser Annealing of Polycrystalline Silicon", L. Gerzberg, A. Gat, K. F. Lee, J. F. Gibbons, J. Peng, T. J. Magee, V. R. Deline, and C. A. Evans, Jr., (Submitted for publication to the Electrochemical Society).

Continuous-wave argon laser annealing and recrystallization of polycrystalline silicon is investigated as a function of laser power in samples implanted with arsenic and boron. The analysis is based on optical microscopy, TEM, SIMS, and Hall measurements. The data obtained reveal three distinct regimes of laser processing:
(1) a low power regime, where the anneal is performed without melting, with no dopant redistribution and with dopant activation similar to thermal annealing; (2) a medium power regime, with moderate dopant

redistribution occurs, probably as a result of partial melting through the layer, and (3) a high power regime, where the melt reaches the underlying amorphous oxide. Large grains are then observed, with the accompanying characteristics of high mobility, complete dopant redistribution, and decreased surface roughness.

Paper No. 3.

"Resistivity Reduction in Heavily Doped Polycrystalline Silicon Using CW-Laser and Pulsed Laser Annealing", T. Shibata, K. F. Lee, J. F. Gibbons, T. J. Magee, J. Peng and J. D. Hong, (Submitted for publication to Journal of Applied Physics).

The resistivity reduction in heavily doped polycrystalline Si by laser annealing and its increase during subsequent heat processing have been studied. Both cw and pulsed lasers are used and the results are compared. In both cases laser annealing reduces the resistivity of doped films by a factor of 2-3 compared to the furnace annealing. A limited resistivity increase is observed in all laser-annealed samples during subsequent thermal annealing, with the final values for resistivity being lowest for cw-laser annealed Si. The subsequent annealing behaviour observed for cw and pulsed laser annealed Si is interpreted in terms of the different grain structures found in these films. It is demonstrated by TEM studies that the resistivity instability is caused by the precipitation of dopants in the form of rod shaped structures localized at the grain boundaries as well as within the crystallites.

Paper No. 4.

"Resistivity Changes in Laser-Annealed Polycrystalline Silicon During Thermal Annealing", T. Shibata, H. Lizuka, S. Kohyama, and J. F. Gibbons, Applied Physics Letters 35, 1, (July 1, 1979).

Polycrystalline silicon layers heavily doped with phosphorus or arsenic were irradiated with a Nd: YAG pulsed laser beam. A 40-50% reduction in sheet resistivity was obtained by laser annealing. However, during subsequent heat treatments the resistivity increased to a value which was higher than the initial value before the laser anneal. The instability of the resistivity is tentatively explained by reprecipitation of dopants both within the grains and at the grain boundaries.

Paper No. 5.

"Crystal Structure and Thermal Oxidation of Laser-Recrystallized Polycrystalline Silicon", T. I. Kamins, K. F. Lee, and J. F. Gibbons, Applied Physics Letters 36, 7, (April 1, 1980).

Laser-recrystallized polycrystalline silicon exhibits a weak <111> preferred orientation, in contrast to the strong <110> texture seen in fine-grain poly-silicon. The oxide thickness thermally grown on laser-recrystallized poly-silicon is much greater than that on fine-grain poly-silicon when both are heavily phosphorus doped but is approximately the same when both films are lightly doped.

Paper No. 6.

"Charges at a Laser-Recrystallized-Polycrystalline-Silicon/Insulator Interface", T. I. Kamins, K. F. Lee, and J. F. Gibbons, IEEE Electron Device Letters, Vol. EDL-1, No. 1, (January 1980).

Capacitance-voltage characteristics have been measured to determine and interface properties at the back surface of a layer of laser-recrystallized polycrystalline silicon. The interface between the recrystallized poly-silicon and an underlying oxide layer can be characterized by an effective fixed-charge density and a fast-state density, both in the low-to-middle-10^{11} cm^{-2} range. Charge trapping at poly-silicon/silicon-nitride interface precludes the determination of a meaningful value of interface charge.

Paper No. 7.

"Interface Charges Beneath Laser-Annealed Insulators on Silicon", T. I. Kamins, K. F. Lee, and J. F. Gibbons, Solid-State Electronics Vol. 23, pp. 1037-1039 (1980).

Laser annealing of a thermally grown, silicon-dioxide layer reduces an initially high fixed-charge density. Similar annealing of a silicon-nitride-covered silicon wafer does not markedly improve the interface characteristics. Laser melting and recrystallization of polycrystalline silicon above a thermally grown oxide does not appreciably increase the interface charges at the underlying silicon-dioxide/single-crystal-silicon interface.

Paper No. 8.

"Thin Film MOSFET's Fabricated in Laser-Annealed Polycrystalline Silicon", K. F. Lee, J. F. Gibbons, K. C. Saraswat, and T. I. Kamins, Applied Physics Letters 35, 2, (July 15, 1979).

Both depletion- and enhancement-mode MOSFET's have been fabricated with the active transistor channels in laser-annealed polycrystalline-silicon films. A dose of 3×10^{12} $^{31}P/cm^2$ was implanted at 100 keV into 0.5-μm-thick poly-silicon films for the depletion-mode device, and a dose of 3×10^{11} $^{11}B/cm^2$ was used for the enhancement-mode device. The transistors fabricated in the poly-silicon films show electrical characteristics comparable to those of devices in single-crystal silicon. In the depletion-mode device, an electron mobility of ~ 450 $cm^2/Vsec$ was obtained, and approximately 80% of the phosphorus was electrically active. The surface mobility of electrons was about 340 cm^2/V sec in the enhancement-mode device, and a threshold voltage of approximately 2.5 V was obtained.

Paper No. 9.

"Silicon-On-Insulator M.O.S.F.E.T.S Fabricated on Laser-Annealed Polysilicon on SiO_2", A. F. Tasch, T. C. Holloway, K. F. Lee, and J. F. Gibbons, Electronics Letters, Vol. 15, No. 14, (July 5, 1979).

N-channel-enhancement and light-depletion-mode m.o.s.f.e.t.s have been fabricated on laser-annealed 0-5 μm polysilicon films, deposited on 1 μm of SiO_2 grown on single-crystal silicon substrates. Threshold voltages of 0·35-0·45 V and -0·5--0·7 V and surface mobilities of 170 cm^2/Vs and 215 cm^2/Vs were obtained n the enhancement and depletion devices, respectively. These results compare favourably with values realised in silicon-on-sapphire (s.o.s) and bulk N-m.o.s. devices. In addition, the measured source-drain leakage currents match the best reported values for s.o.s. device.

Paper No. 10.

"A Monolithic Integrated Circuit Fabricated in Laser-Annealed Polysilicon", T. I. Kamins, K. F. Lee, J. F. Gibbons, and K. C. Saraswat, IEEE Transactions on Electron Devices, Vol. ED-27, No. 1, (January 1980).

An integrated-circuit (IC) fabrication process has been used to construct small-geometry MOS transistors and a ring oscillator with the active transistor channels in a thin layer of laser-annealed poly-silicon. Both enhancement-mode and depletion-mode n-channel, silicon-gate transistors have been fabricated with dimensions compatible with high-performance MOS technology (gate lengths as short as 3 μm). A modified LOCOS process was used to fabricate the devices so that each transistor was contained within a pocket of silicon completely isolated from adjacent elements by dielectrics. The transistors were well behaved, with mobilities approaching those in single-crystal silicon, reasonably abrupt subthreshold characteristics, and low leakage current. An operating, nine-stage ring oscillator was also fabricated, and its behavior suggests the approach for further optimization. The technology offers the possibility of high-performance IC's on potentially inexpensive substrates, as well as the possibility of additional levels of devices on monolithic silicon IC's.

Paper No. 11.

"Ring Oscillators Fabricated in Laser-Annealed Silicon-On-Insulator", H. W. Lam, A. F. Tasch, Jr., T. C. Holloway, K. F. Lee, and J. F. Gibbons, IEEE Electron Device Letters, Vol. EDL-1, No. 6, (June 1980).

Both seven and eleven stage n-MOS ring oscillators with 6 μm channel length have been successfully fabricated in scanning. CW argon laser-annealed polycrystalline silicon islands, which are defined prior to the laser annealing step, on oxide substrates. The ring oscillators, which have a fan-out of three, have a switching delay per stage of 58 nsec and a power-delay product of about 7 pJ operating at a supply voltage (V_{DD}) of 5 volts and switching between V_{DD} and ground. The most serious difficulty encountered during circuit fabrication was the deformation of the silicon islands resulting from laser annealing with extensive laser power density.

Paper No. 12.

"Micrometre-Gate M.E.S.F.E.T.S. on Laser-Annealed Polysilicon", J. Barnard, J. Frey, K. F. Lee, and J. F. Gibbons, Electronics Letters, Vol. 16, No. 8, (April 10, 1980).

Schottky-barrier field-effect transistors (m.e.s.f.e.t.s) have been fabricated on uniformly doped laser-annealed polycrystalline silicon deposited on a silicon nitride insulator. The devices, which had aluminium Schottky-barrier gates and diffused n^+ sources and drains but nonoptimised channel profiles, had about 65% the g_m values of similar but optimised devices made on s.o.s. layers. Performance of these devices is considered adequate for certain innovative integrated-circuit technologies.

Paper No. 13.

"One-Gate Wide CMOS Inverter on Laser-Recrystallized Polysilicon", J. F. Gibbons and K. F. Lee, IEEE Electron Device Letters, Vol. EDL-1, No. 6, (June 1980).

A CMOS inverter having a single gate for both n and p channel devices has been fabricated using bulk silicon for the p channel device and a laser-recrystallized silicon film for the n channel device. The fabrication details and dc electrical performance of this device are described.

Paper No. 14.

"CW Laser Recrystallization of <100> Si on Amorphous Substrates", J. F. Gibbons, K. F. Lee, T. J. Magee, J. Peng, and R. Ormond, Applied Physics Letters 34, 12, (June 15, 1979).

A polycrystalline silicon film 0.55 μm thick was deposited in a low-pressure CVD reactor on a Si_3N_4 substrate. Islands of various sizes (2x20 μm up to 20x160 μm) were prepared by standard photolithographic techniques. Laser annealing was then performed under conditions which are known to cause an increase in grain size from ~ 500 Å to long narrow crystals of 2x25 μm in a continuous polysilicon film. These same conditions were found to produce single-crystal <100> material in the (2x20 μm) islands. However, 25x25-μm and 20x160-μm islands remain polycrystalline after the laser scan.

Paper No. 15.

"LPE Growth of Silicon From Poly Si/Si Structure Using CW Argon Laser", S. Minagawa, K. F. Lee, J. F. Gibbons, T. J. Magee, and R. Ormond, Journal of Electrochemical Society, Vol. 28, No. 4, (April 1981).

Epitaxial layers were grown by melting the surface of polysilicon/silicon structure with a scanning cw argon laser beam. Topographical features and crystalline perfection assoicated with the laser induced recrystallization were investigated by transmission electron microscopy (TEM) and optical microscopy. The regrown layers obtained were relatively free of defects, as revealed by TEM analysis. Large concentrations of dislocation lines and twinning zones were not detected in these studies: however dense dislocation networks were observed in the substrate beneath the epitaxial layer.

Paper No. 16.

"Lateral Epitaxial Recrystallization of Deposited Silicon Films on Silicon Dioxide", T. I. Kamins, T. R. Cass, C. J. Dell'Oca, K. F. Lee, R. F. W. Pease, and J. F. Gibbons.

A scanning CW argon laser has been used to epitaxially recrystallize silicon films deposited over exposed regions of single-crystal silicon substrates and cause the lateral extension of these epitaxial regions into the portions of the silicon film deposited over oxide-covered regions of the substrate. Planar and cross-sectional transmission electron miroscopy were used to investigate the microstructure, which is consistent with melting and liquid-phase regrowth.

Paper No. 17.

"Properties of MOSFETS Fabricated in Laser-Annealed Polysilicon Films", K. F. Lee, J. F. Gibbons, K. C. Saraswat, T. I. Kamins, H. W. Lam, A. F. Tasch, Jr., and T. C. Holloway, presented at Materials Research Symposium, Cambridge, Mass., November 27-30, 1979. To be published in Proceedings.

Enhancement-mode and depletion-mode MOSFETs of 3 μm gate lengths have been fabricated with the transistor channels in thin films of polycrystalline silicon annealed with a scanning cw argon laser. Device

performance of the transistors was comparable to those fabricated in single crystal silicon. A nine-stage ring oscillator was also fabricated. Minority carrier generation lifetime of the order of 10^{-9} sec. was measured in the laser-annealed polysilicon.

Paper No. 18.

"CW Laser-Recrystallized Polysilicon as a Device-Worthy Material", J. F. Gibbons, presented at Materials Research Symposium, Boston, Massachusetts, November 16, 1980. To be published in Proceedings.

The basic crystallographic and electronic properties of cw laser recrystallized thin polysilicon films are presented and shown to be suitable for fabrication of MOSFET devices. Devices and simple integrated circuits fabricated to explore the potential of this material have electrical characteristics similar to devices fabricated on single crystal material and offer significant promise for future applications.

Paper #1

"CW Laser Anneal of Polycrystalline Silicon: Crystalline Structure, Electrical Properties".

Paper #2

"Effect of Power Level in CW Laser Annealing of Polycrystalline Silicon".

Paper #3

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"CW Laser-Recrystallized Polysilicon as a Device-Worthy Material".

cw laser anneal of polycrystalline silicon: Crystalline structure, electrical properties

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(Received 15 June 1978; accepted for publication 16 August 1978)

0.4-μm-thick polycrystalline silicon deposited in a low-pressure CVD reactor was implanted with B to a dose of $5\times10^{14}/cm^2$ and then irradiated in a cw laser scanning apparatus. The laser annealing produced an increase in grain size from ~500 Å to long narrow crystals of the order of $\sim25\times2$ μ, as observed by TEM. Each grain was found to be defect free and extended all the way to the underlying Si_3N_4. Electrical measurements show 100% doping activity with a Hall mobility of about 45 cm^2/V sec, which is close to single-crystal mobility at the same carrier concentration. Thermal annealing produces material with an average grain size of 1000 Å and a resistivity higher by a factor of 2.2 than that obtained with the laser anneal. Laser annealing performed after a thermal anneal reduces the resistivity to approximately the same value obtained by laser annealing only.

PACS numbers: 72.80.Cw, 81.40.Rs, 72.20.Fr, 81.40.Ef

Recent literature describes the use of both pulsed and cw laser irradiation to anneal ion implantation damage in semiconductors[1–9] and to recrystallize amorphous semiconductor films. In particular, the present authors have shown[5–7] that, using a cw-scanned system, laser annealing of implantation-amorphized crystalline silicon completely restores crystalline perfection while activating the implanted dopants. Another advantage which is thus far unique to the continuous scan is the lack of diffusion of impurities during the anneal process[6] in the case of annealing ion-implanted single-crystal silicon.

Most studies to date have been concerned with the use of the cw laser system to anneal damaged single crystals or shallow amorphized layers on top of single-crystal material, though Laff and Hutchins[9] also report on the use of a cw laser for recrystallization of CVD silicon films on silica.

In this paper we investigate the interaction of a continuous laser scan with polysilicon layers deposited on top of amorphous substrates such as Si_3N_4 and SiO_2. We have found that the major structural effects of the laser scan is to increase the grain size of the polycrystalline material. Electrical measurements performed on thermal, laser, and laser-after-thermal annealed samples show that essentially 100% electrical activation of the implanted dopant is obtained. Carrier mobilities that are consistent with bulk values for the given doping level are also achieved.

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The polysilicon samples used were obtained by low-pressure chemical vapor deposition (LP CVD) of silicon. Polysilicon layers approximately 0.4 μm thick were deposited in a commercial Tempress reactor. The substrates used were crystalline Si onto which had been deposited a 1000-Å layer of Si_3N_4.

After deposition of the poly, the wafers were ion implanted with $5 \cdot 10^{14}$ B^+ cm^{-2} at 60 keV at room temperature. After implantation, the wafers were cut into a set of 5 · 5-mm samples. Several samples were subjected to a 1100 °C 30-min thermal anneal in flowing dry N_2 to provide standards of comparison for the laser-annealed samples.

The laser-annealed samples were irradiated in the scanning apparatus described in Ref. 5. A cw argon laser (Spectra Physics Model 171-09) was used in the multiline mode. The laser output was focused by a 136-mm lens onto a sample placed in the focal plane of this lens. Two perpendicular mirrors driven by galvanometers were used to scan the laser spot across the sample in the x and y directions. The calculated laser beam width at the $1/e$ points for a TEM_{00} mode and a wavelength of 5145 Å is 37.2 μ. However, in these experiments the laser was used in the multiline mode with a full aperture. This may cause exitation of higher modes than TEM_{00} and will increase the beam width so that 37.2 μ can only be considered as a lower estimate of the actual beam size.

The samples were held to a brass sample holder by a vacuum chuck during annealing. The holder was heated by an ac heating coil, and its temperature was monitored with a thermocouple mounted 1 mm from the backside of the sample. A constant x-scan rate of 12.5 cm/sec was used. The laser power and the backside temperature were varied to investigate their effect on structural and electrical properties. Samples annealed by laser only were held at a backside temperature of 250 °C with a laser power of 14 W, while those that were subjected to laser-after-thermal annealing were held at 350 °C and the laser power was 11 W. It was found that the annealed

FIG. 1. Surface structure (SEM) of one laser scan line on polysilicon.

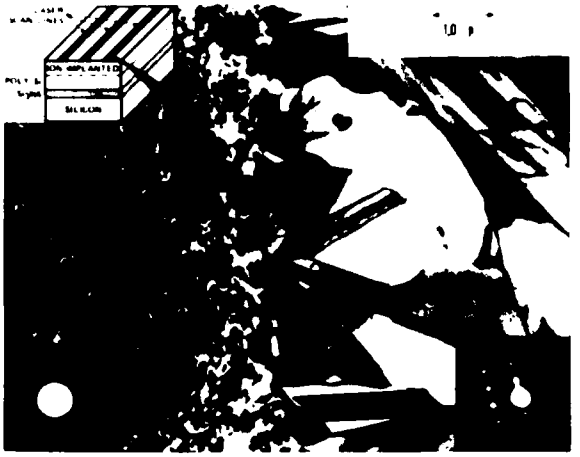

FIG. 2. Transmission electron micrograph of ion-implanted laser-annealed poly-Si film at boundary of laser scan line; insets show selected area diffraction patterns characteristic of each region.

line width, which was measured optically, was approximately 40 μ and had little sensitivity to the x-scan rate.

For TEM structural analysis, separate anneal lines were obtained by stepping the x scan by 100 μ after each x scan. For electrical measurements, stepping of the y scan was reduced to 25 μ so that each line overlapped the previous line by ~40%. In each case, several samples were annealed to identify any possible statistical fluctuations.

Most of the samples reported on were boron doped directly by ion implantation. However, a single annealing experiment was performed on a conventional heavily phosphorous-doped polysilicon material used in the silicon gate process. Samples for these experiments consisted of polysilicon that had been deposited directly on 1000 Å of SiO_2. The deposition was done in a LP CVD reactor and gave a layer thickness of 0.57 μ. After deposition, the wafers were thermally diffused to obtain a P concentration of 1.5×10^{20} cm^{-3}. Electrical measurements made on this material before and after laser annealing are also reported below.

Laser-annealed lines were examined by SEM to investigate their surface structure. Figure 1 shows a single laser line surrounded by unannealed poly. The laser-annealed region is characterized by a darker appearance in the SEM (in an optical microscope, the annealed line is brighter). The streaks in the annealed area are pointed in the direction of the scan. The long lines in the center of the annealed area correlated with TEM results which show long narrow single-crystal grains that extend all the way to the silicon nitride. Comparing the two regions in Fig. 1, we conclude that the laser scan decreases the microscopic roughness of the surface.

We used transmission electron microscopy and diffraction analysis to investigate the relative structure of control, thermally annealed, and laser-annealed samples. Samples were jet thinned from the back surface before examination with the TEM.

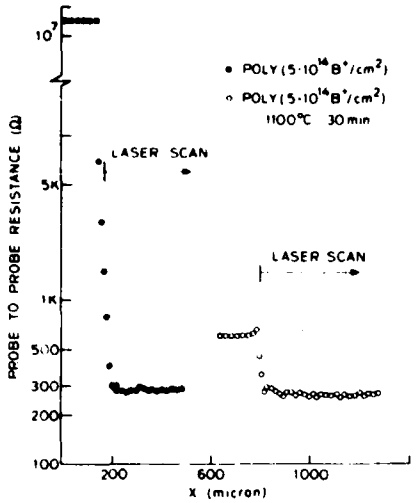

FIG. 3. Surface spreading resistance measurements done on 5×10^{14} B^+/cm^2 implanted polysilicon. Samples were subjected to laser and laser-after-thermal anneal.

Examination of control samples showed a fine-grained structure with an average grain size ≈550 Å. In all samples, we observed a significant number of dislocations and stacking faults within individual grains. After an 1100 °C 30-min thermal anneal of the implanted samples, the average grain size increased to ~1060 Å. Defects remained within grains of the annealed film in the form of dislocation loops, stacking faults, and dislocation lines, implying that conventional high-temperature annealing did not effectively remove residual defects in the polycrystalline layer.

Figure 2 shows a bright-field transmission electron micrograph of a boron-implanted laser-annealed structure at the boundary of the laser scan line. Selected area diffraction patterns obtained within the unscanned area (left inset, Fig. 2) show the anticipated ring pattern with no observable change from control samples. Within the laser-scanned region, however, there is dramatic evidence of crystal growth, as observed in the right portion of Fig. 2. Columnar crystallites extending from the laser-scan boundaries to the interior of the scanned region are noted in all samples examined. The crystallites are typically developed at an angle to the laser scan boundaries, producing a chevron structure in the direction of the laser line scan. In the center of the laser-scan region, crystallites are long and narrow and are aligned parallel to the laser line with maximum length ~32 μm and an average width of ~2 μ. Selected area diffraction patterns obtained within the scanned section (right inset of Fig. 2) show no evidence of fine-grained polycrystalline structure remaining in the region. However, the columnar crystallites display a number of crystal orientations with no indication of a preferred orientation.

Diffraction patterns obtained using the entire thickness of the polycrystalline film showed only single-crystal patterns and Kikuchi lines, with no detectable evidence of (fine grained) polycrystalline diffraction rings. This data suggested that the columnar crystallites were continuous structures extending from the Si_3N_4 interface to the surface of the film. To further substantiate this observation, we then removed a portion of the front surface by chemical thinning to produce a 1000-Å-thick layer at the Si/Si_3N_4 interface. Diffraction patterns again showed only single-crystal spots, thereby verifying that columnar growth extends throughout the thickness of the Si film.

TABLE I. Electrical properties and structure comparison of different laser anneal condition on 5×10^{14} B^+/cm^2 implanted polysilicon.

Anneal condition	As-implanted	Thermal anneal	Laser anneal	Laser after thermal anneal
Grain size	300—600 Å	900—1200 Å	$\overline{25}\times\overline{2}$ μ	$\overline{25}\times\overline{2}$ μ
Sheet resistivity (Ω/□)	12.5 MΩ/□	623 Ω/□	269 Ω/□	260 Ω/□
Sheet carrier concentration (cm^{-2})	unmeasurable	4.7×10^{14} cm^2	5.2×10^{14} cm^2	5.17×10^{14} cm^2
Mobility (cm^2/V sec)	unmeasurable	24	44.5	46

Electrical properties were measured on as-implanted, thermally annealed, laser-annealed, and laser-after-thermal annealed samples. The properties measured included both two-point probe spreading resistance and Van der Pauw measurements, from which carrier concentration and Hall mobility were calculated. The spreading resistance was measured on samples which had overlapping laser line scans over one-half of the wafer. The 100-μ spaced probes were scanned from the unannealed to the laser-annealed area. The probe-to-probe resistance is shown in Fig. 3. A one-to-one correlation was observed between the spreading resistance reading and the sheet resistivity. Figure 3 shows that the sheet resistivity of the samples dropped from an as-implanted value of 12.5 MΩ/□ to 625 Ω/□ after thermal anneal. A sheet resistivity of 280 Ω/□ was observed when laser annealing was performed directly on the as-implanted samples, while samples which were thermal annealed first and then annealed by laser showed a slightly lower resistivity of 260Ω/□.

Resistivity measurements were also performed using a Van der Pauw configuration. Measurements were performed with the probes placed at the four corners of the samples and then repeated with the probe connections rotated by 90°. Based on the two measurements, a correction factor was calculated to account for geometrical asymmetry. The difference in the two readings which can be explained by geometrical asymmetry was up to 25% in the case of thermal-annealed samples. Distinctive differences of up to 400% were observed in the samples subjected to laser anneal. A summary of the measurements results, together with the corresponding grain size measured by TEM, is given in Table I.

The measured sheet carrier concentration was close to the implanted dose of 5×10^{14} cm^{-2} in the case of laser-annealed samples with or without thermal anneal-

ing, and 4.7×10^{14} cm^{-2} in thermal-annealed samples. A Hall mobility of 24 cm^2/V sec was obtained in thermally annealed samples, compared to a value of 46 cm^2/V sec in the laser—after—thermal-annealed case. It is seen from Table I that the reduction in sheet resistivity and the increase of mobility correlate with a significant increase of grain size. The resistivity measured on the heavily P-doped polysilicon obtained by thermal diffusion was 31 Ω/□ after doping and 13.8 Ω/□ after laser anneal. This is accompanied by an increase of Hall mobility from 24.8 to 43.3 cm^2/V sec. The correlation between the increase in grain size and the changes in electrical properties is in direct agreement with the grain-boundary trapping model proposed by Kamins[10] and confirmed by Seto.[11] The observed 200—400% asymmetry in the resistivity measures parallel to and across the annealed lines is explained by the directional nature of the crystallized grains. We believe that this effect causes the observed asymmetry in the Van der Pauw measurements.

The authors are indebted to ARPA (Contract No. MDA903-78-C0128) for support of the work reported here, to Dr. R. Reynolds for his personal interest, and to Dr. G. Parker (Intel Corporation) for supplying the wafers for the experiments. We would also like to thank Stan Warner for the design and construction of the temperature-controlled sample holder and Nancy Latta for assistance in sample preparation.

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EFFECT OF POWER LEVEL IN CW LASER ANNEALING OF POLYCRYSTALLINE SILICON

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ABSTRACT

Continuous-wave argon laser annealing and recrystallization of polycrystalline silicon is investigated as a function of laser power in samples implanted with arsenic and boron. The analysis is based on optical microscopy, TEM, SIMS, and Hall measurements. The data obtained reveal three distinct regimes of laser processing: (1) a low power regime, where the anneal is performed without melting, with no dopant redistribution and with dopant activation similar to thermal annealing; (2) medium power regime, with moderate dopant redistribution occurs, probably as a result of partial melting through the layer, and (3) a high power regime, where the melt reaches the underlying amorphous oxide. Large grains are then observed, with the accompanying characteristics of high mobility, complete dopant redistribution, and decreased surface roughness.

I. INTRODUCTION

The interest in CW laser annealing of polycrystalline silicon (polysilicon) has increased substantially because of its potential use in device and circuit applications. CW laser annealing has been applied for diode-array fabrication [1], and amorphous silicon has been converted into polycrystalline silicon for photovoltaic applications [2]. The reduction of polysilicon resistivity in interconnection lines was proposed [3], and resistivity control has been improved through CW laser annealing [4]. MOS transistors have been fabricated in laser-annealed polysilicon [5]. In these studies, the polysilicon layer was completely melted to achieve large grains and, in some applications [4], low-power annealing was also investigated. The effect of laser power

on the annealing process and related dopant redistribution, however, has not been reported.

This paper describes the annealing of polysilicon irradiated by a CW argon laser, with emphasis on the relation between laser power and surface morphology, crystal structure, dopant distribution, and electrical properties. Three power levels (low, medium, and high) have been identified, with the general effects described in Fig. 1. It can be seen that complete dopant activation already occurs at low-power levels. A moderate grain-size increase with dopant redistribution is observed at higher irradiation intensities. In the medium-power range, partial melting causes a gradual growth in grain size and some dopant redistribution. High-power anneals result in complete layer melting with its attendant drastic increase in grain size, uniform dopant redistribution, and sharp reduction in electrical resistivity. In what follows we give further details on the process and also describe features that are observed where single line annealing is compared to annealing obtained with overlapped scans.

II. EXPERIMENTAL SETUP AND RESULTS

0.57 μm polycrystalline silicon (polysilicon) was deposited in a low-pressure CVD reactor on top of 1000 Å of thermally grown silicon dioxide. After deposition, the wafers were ion-implanted with either As^+ at 170 keV with a $5 \times 10^{15}/cm^2$ dose or B^+ at 100 keV with a $5 \times 10^{14}/cm^2$ dose. They were then cut into 5 x 5 mm samples.

The samples were irradiated in the scanning apparatus described in Ref. 6. A CW argon laser was operated in the multiline mode, with its output focused by a 136 mm lens onto a sample placed in the focal

plane of that lens. Two perpendicular mirrors driven by galvanometers scanned the laser spot across the sample in the x and y directions. The laser beamwidth was estimated to be 37.2 μm at the 1/e points for a TEM_{00} mode and a wavelength of 5145 Å. However, because the laser was used in the multiline mode with a full aperture which may excite modes higher than TEM_{00} and increase the beam-width, 37.2 μm can only be considered as a lower estimate of the actual size.

The samples were held to a brass sample holder by vacuum during annealing. The holder was heated by an ac coil, and its temperature was monitored by a thermocouple mounted 1 mm from the back surface of the sample. A constant x-scan rate of 12.5 cm/sec was selected.

These conditions remained constant; the only parameters that varied were substrate temperature, laser power, and the distance between two adjacent lines (amount of overlap). It was found to be advantageous to increase the substrate temperature to 350°C. The laser power was varied in 1 W increments from 5 W up to approximately 8.5 W for the boron samples and 13 W for arsenic. The polysilicon was stripped away to expose the underlying oxide for larger laser power levels.

Optical micrographs of the annealed lines in the polysilicon showed a linewidth of 40 μm. Because this investigation was directed toward applications in device processing, it was desirable to cover large areas uniformly. Stepping in the y direction was 25 μm so that each line overlapped the previous one by 40 percent.

It should be emphasized that this is not the only set of optimal annealing conditions; a different laser spot, scan rate, and substrate temperature can yield similar results.

Structure Analysis

For both the arsenic- and boron-implanted samples, the laser power was varied and the surface was examined through a Nomarski interference contrast microscope and SEM. Two distinct regions having a sharp transition were observed. The arsenic samples at low and medium power (5 and 9 W respectively) displayed no significant change in surface morphology (Fig. 2a,b). Above 10 W, distinct lines were apparent in the non-overlapping sample with the microstructure inside the line pointing in the direction of the scan. Figure 2c is a SEM micrograph of the high-power region, showing the directionality in the line, smoothing of the original fine surface roughness and the formation of large surface structures. The surface smoothing of small structures, through laser annealing, has led others to investigate the quality of oxide thermally grown on the polysilicon surface [7,8], as well as the orientation of the various crystallites [8].

Grain size was analyzed through transmission electron microscopy (TEM) and diffraction analysis. Samples were jet thinned from the back surface before examination. Figure 3 presents TEM micrographs of boron-implanted polysilicon irradiated with single and overlapping lines. The long crystallites in the single-line scan are characteristic of the high-power region. These crystallites are continuous structures extending from the SiO_2 interface to the surface of the film [3]. The difference between the single and overlapping lines is explained in Section III in terms of thermal-conductivity variations.

Figure 4 is a series of TEM photomicrographs of arsenic-implanted polysilicon laser annealed at low-, medium-, and high-power levels. The as-deposited samples display fine-grained structure with an average

grain size of approximately 550 Å. The laser-annealing results obtained at 7 and 9 W do not deviate significantly from the as-deposited sample. A sharp change is observed at the high-power level of 10 W and above, as evidenced by the 15 to 25 μm grain size in the 11 W sample. The nature of this high threshold and its implications are discussed in Section III.

Further understanding of the process can be gained from the plots of average grain size vs laser power of the boron- and arsenic-implanted samples in Figs. 5 and 6. In Fig. 5, the grain size of the boron-implanted sample is seen to increase monotonically in the medium-power range of 6 to 8 W. The transition to the high-power level occurs only in the single-line scan when the power is greater than 9 W. In this narrow window (8 to 9 W), grain size increases from 1 to 10 μm and, at 11 W, it grows to 20 μm.

Figure 6 is a plot for arsenic-implanted polysilicon. As was the case for the boron-implanted samples, grain size increases monotonically at 6 to 9 W. The transition to the high-power level occurs between 9 and 10 W, above which a 20 μm grain size is commonly observed. In contrast to boron, however, there is no significant difference between the single and overlapping lines.

Dopant Distribution

Secondary ion-mass spectrometry (SIMS) was used to obtain dopant-profile measurements. Oxygen primary ion-bombardment and positive secondary ion-mass spectrometry (B^+ and As^+) were employed, using the CAMECA IMS-3f ion microanalyzer. The boron profiles were determined through standard depth profiling; however, sensitive measurements of the As profiles required secondary ion initial kinetic discrimination

to reduce the amount of $(^{30}Si^{29}Si^{16}O)^+$ detected at the same nominal mass as $^{75}As^+$. This analysis was sufficient to determine the As detection limits of 3 to 5 $x10^{18}$ atoms/cm^3. As can be seen in Fig. 7, the high oxygen content of SiO_2 and the minor surface-charging effects produce an anomolously high mass-75 intensity that misrepresent the true arsenic content in the oxide region. This problem, however, did not hinder the measurements in the poly-Si layer.

In the 6 W sample in Fig. 7, the dopants did not move from their as-implanted position. The profile is approximately Gaussian and can be adequately predicted from Lindhard-Scharff-Schiott (LSS) range calculations [9]. Increased laser power results in deeper impurity penetration into the polysilicon.

When the power level was raised to 11 W, the dopant profiles became flat throughout the polysilicon layer. The inserts in Fig. 7 are the TEM micrographs measured at 9 and 11 W. It can be seen that, although partial melting occurred at 9 W, the grains are still small ($\sim$ 0.3 μm); their growth is considerable ($\sim$ 20 μm) only when the melt front reaches the underlying oxide layer.

Figure 8 plots the boron concentration in the polysilicon layer after laser irradiation. The artificial boron intensity observed in the oxide could be the result of a change in the ionization yield of the boron atoms implanted in the oxide. This boron redistribution further substantiates the theory of surface melting. The 5 W level is identical to the as-implanted distribution and, again, it can be calculated by LSS theory. As the power is increased, the region wherein the boron profile is flat also increases. At 8.5 W, 0.2 μm of the polysilicon is molten and the dopants redistribute in the molten region whereas

their remaining positions are unchanged.

For boron-implanted samples, power cannot be raised beyond 8.5 W because the polysilicon would peel off from the underlying oxide.

Electrical Properties

Sheet resistivity, carrier concentration, and Hall mobility were measured as a function of laser power by means of a Van der Pauw configuration.

Figure 9 plots the sheet resistance, mobility, and active-carrier concentration (N_s) in the arsenic-implanted laser-annealed polysilicon. The most important observation is that the carrier concentration is fixed at an approximate level of 3.5×10^{15} cm^{-2} (implantation dose was 5×10^{15} cm^{-2}), independent of laser power. This graph also shows that, even at the lower power level (5 to 6 W) for which the SIMS data indicate no diffusion, the dopants are almost all active. This is in agreement with our earlier work on CW annealing of ion-implanted single crystals wherein the implanted dopant in the solid-phase state can be activated with no diffusion [10]. At the medium-power level (6 to 9 W), sheet resistance decreases because of greater mobility and with no change in the number of active carriers. This increase in mobility drops at 9 W and, as power is raised to 10 W, a sharp transition to the high-power region is accompanied by a rapid rise in mobility. In this region, as power is raised to 10 to 12 W, the trend toward greater mobility decreases, but with no effect on N_s.

In the boron samples, the laser power could not be raised above 8.5 W without peeling the polysilicon from the oxide. As a result, the high-power region where mobility approaches that of single-crystal silicon is missing in Fig. 10. It is important to note that, in an

earlier experiment [3] where the polysilicon was deposited over Si_3N_4 with the same boron dose at 11 W, a grain size of approximately 25 μm, resistivity of 269 Ω/□ , and mobility of 44.5 $cm^2/V/sec$ were achieved. This means that, when polysilicon is deposited over nitride, it is possible to reach the high-power level. After the above experiment was performed, the problem of the peeling of the polysilicon from the oxide has been solved. It was observed that by carrying out a 1100°C N_2 anneal for 1 hour immediately prior to the laser annealing the laser power level could be increased without the occurrence of peeling [11].

III. DISCUSSION

The results obtained from the structure analysis, plus dopant distributions and electrical properties, serve as the basis in this section for a proposed explanation for the effect of laser power on polysilicon annealing. The following three laser power levels have been identified (for a 0.57 μm film):

Low Power. This range is characterized by no change in surface morphology, no increase in grain size or dopant redistribution and complete dopant activation with low carrier mobility. Laser heating without melting is responsible for these results, under conditions similar to CW laser annealing of ion-implanted single crystal silicon [10]. A power level of 5 W is characteristic of this region.

Medium Power. When the laser power is raised from 5 to 9 W, the electrical properties in the top layer are changed. Surface roughness increases as does grain size, and dopant diffusion occurs in the top 1000 to 3000 Å. This region is marked by greater mobility, reduced resistivity, and active implanted dopants.

All of these factors suggest that the polysilicon layer begins to melt from the surface downward. Because the actual annealing time is on the order of 1 msec, it is impossible to explain such phenomena with simple solid-state diffusion. If partial melting of the polysilicon at this power level is assumed, and an impurity diffusion coefficient on the order of 10^{-4} cm^2/sec is postulated, it follows that diffusion in the liquid phase is responsible for the dopant redistribution -- a phenomenon closely similar to that observed in pulsed-laser annealing [12,13].

It is important to note that, although melting occurs, no significant change in grain size is observed. This may be explained by a crystallization process that begins in the fine-grained polysilcion substrate that serves as the nucleating layer.

High Power. All electrical properties change in the power range between 9 and 10 W. In this narrow region, there is a significant change in surface structure, a very large increase in grain size (from 1 to 20 μm) a steep rise in mobility, and a uniform dopant distribtuion throughout the layer. Large grains develop when the layer is completely molten all the way to the underlying substrate Complete melting, therefore, is essential for the development of such grains. If samples are lightly doped and complete melting cannot occur without damage to the samples, then large grains will not develop.

In all of the above experiments, the maximum laser power that could be used on the boron-implanted samples was limited to 8.5 W for overlapped scans and 11 W for single scans. Above these levels the polysilicon peels off and the underlying oxide is exposed. This is in contrast to the arsenic-implanted polysilicon, where the maximum power levels were found to be 12 and 13 W for overlapped and non-overlapped scans, respectively. However, if the boron-implanted samples are first thermally annealed, the difference just noted disappears [13]. Furthermore, if the polysilicon is deposited on nitride rather than oxide, the difference between boron and arsenic implanted samples again disappears.

Another interesting phenomenon in the boron-implanted samples is that the critical power (above which polysilicon peels off) is 8.5 W

samples, the corresponding power levels are 12 and 13 W, respectively. An additional effect which could be related to different cooling rates of single and overlapping lines is the different grain size obtained in these two cases in the boron implanted samples (Fig. 5). The difference in cooling rates may be attributed to the low thermal conductivity of fine-grain polysilicon which exists only on one side of the line in the case of overlapping scan. In single line scan the low thermal conductivity material exists on both sides which results in a slower heat extraction than in the previous case. Additional experiments are required, however, to verify the explanations of these phenomena.

IV. SUMMARY

In this paper, the properties of CW laser-annealed polysilicon ion-implanted with boron and arsenic have been reported. Three distinct power levels were identified and correlated with TEM, SIMS, and electrical measurements based on thermal heating/melting of the polysilicon layers. The formation of large columnar crystallites is obtained only when the polysilicon is melted completely to the silicon/insulator interface. The differences between polysilicon deposited over Si_3N_4 and over SiO_2 and the stripping of boron-implanted material have been noted. More work is required to understand the stripping mechanism and thus to achieve a more complete understanding of laser-recrystallized polysilicon.

Acknowledgment

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FIGURE CAPTIONS

Figure 1. Summary of the effects of laser power on the annealing of polysilicon and the corresponding measurement methods.

Figure 2. Surface structure (SEM) of one laser scan line on arsenic implanted polysilicon.

a. Low power (5 W)

b. Medium power (9 W)

c. High power (12 W)

Figure 3 TEM photomicrographs of single and overlapping lines on boron-implanted polysilicon.

Figure 4 TEM photomicrographs of arsenic-implanted laser-annealed samples at the three power levels.

Figure 5 Average grain size of boron-implanted laser-annealed polysilicon as a function of annealing power levels for single and overlapping lines.

Figure 6 Average grain size of arsenic-implanted laser-annealed polysilicon as a function of annealing power levels for single and overlapping lines.

Figure 7 SIMS profile of arsenic-implanted polysilicon after laser annealing at different power levels. Inserts are the corresponding TEMS for 9 and 11 W.

Figure 8 SIMS profile of boron-implanted polysilicon after laser annealing with different power levels.

Figure 9 Sheet resistance, Hall mobility, and total active carriers of 5×10^{15} As^+ implanted in polysilicon with 170 keV and cw laser annealed as a function of laser power.

Figure 10 Sheet resistance, Hall mobility, and total active carriers of 5×10^{14} B^+ implanted in polysilicon with 100 keV and cw laser annealed as a function of laser power.

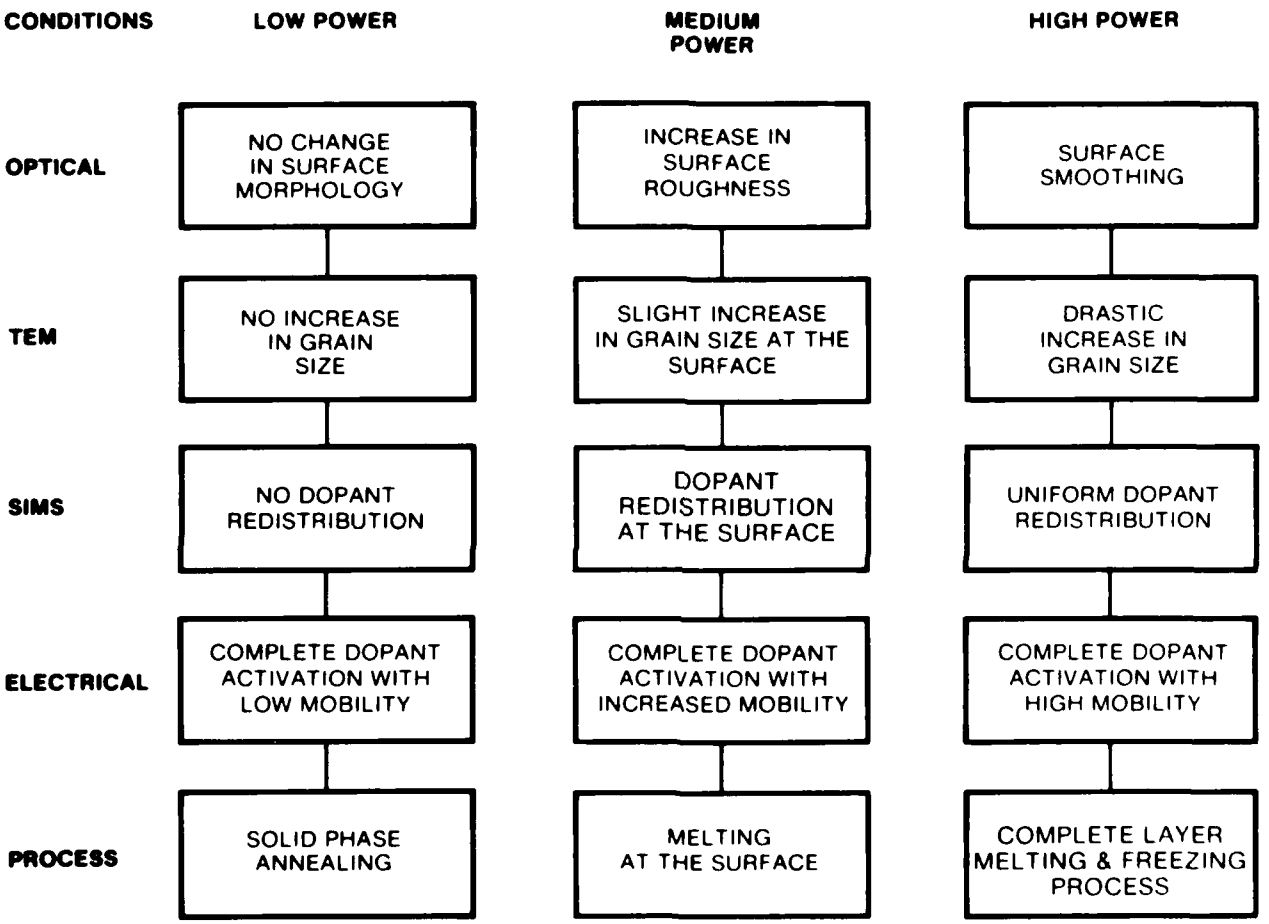

CONDITIONS
LOW POWER
MEDIUM POWER
HIGH POWER
OPTICAL
NO CHANGE IN SURFACE MORPHOLOGY
INCREASE IN SURFACE ROUGHNESS
SURFACE SMOOTHING
TEM
NO INCREASE IN GRAIN SIZE
SLIGHT INCREASE IN GRAIN SIZE AT THE SURFACE
DRASTIC INCREASE IN GRAIN SIZE
SIMS
NO DOPANT REDISTRIBUTION
DOPANT REDISTRIBUTION AT THE SURFACE
UNIFORM DOPANT REDISTRIBUTION
ELECTRICAL
COMPLETE DOPANT ACTIVATION WITH LOW MOBILITY
COMPLETE DOPANT ACTIVATION WITH INCREASED MOBILITY
COMPLETE DOPANT ACTIVATION WITH HIGH MOBILITY
PROCESS
SOLID PHASE ANNEALING
MELTING AT THE SURFACE
COMPLETE LAYER MELTING & FREEZING PROCESS

Fig. 1

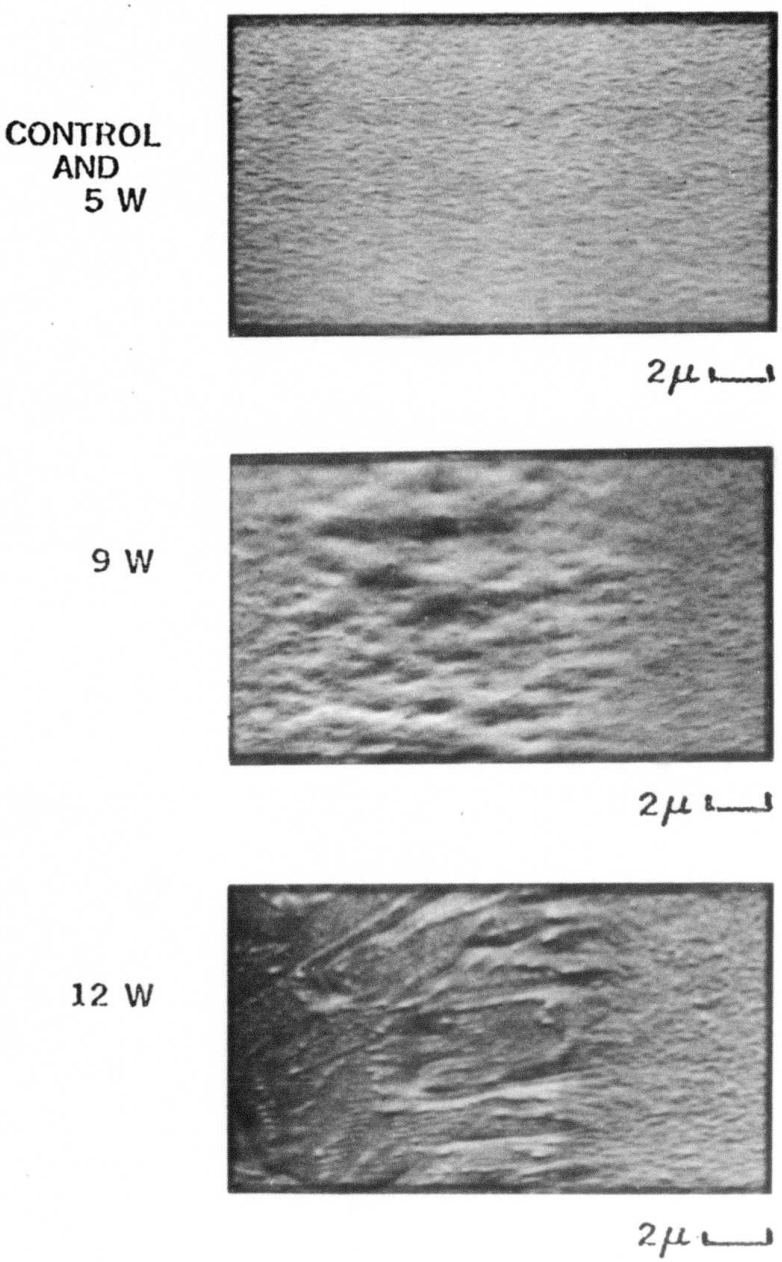
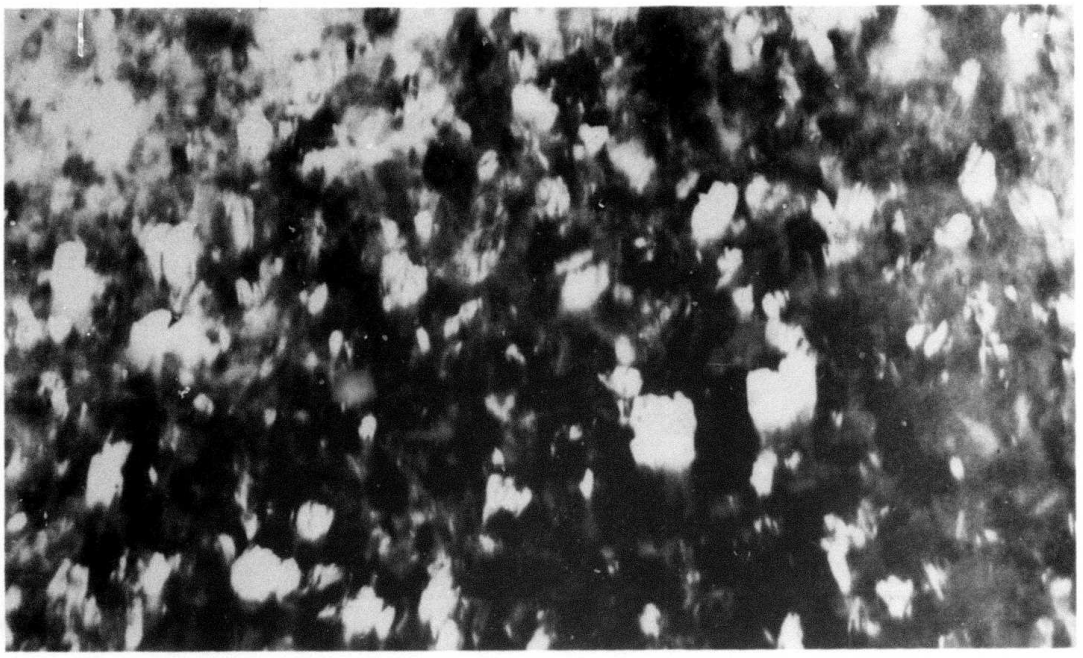
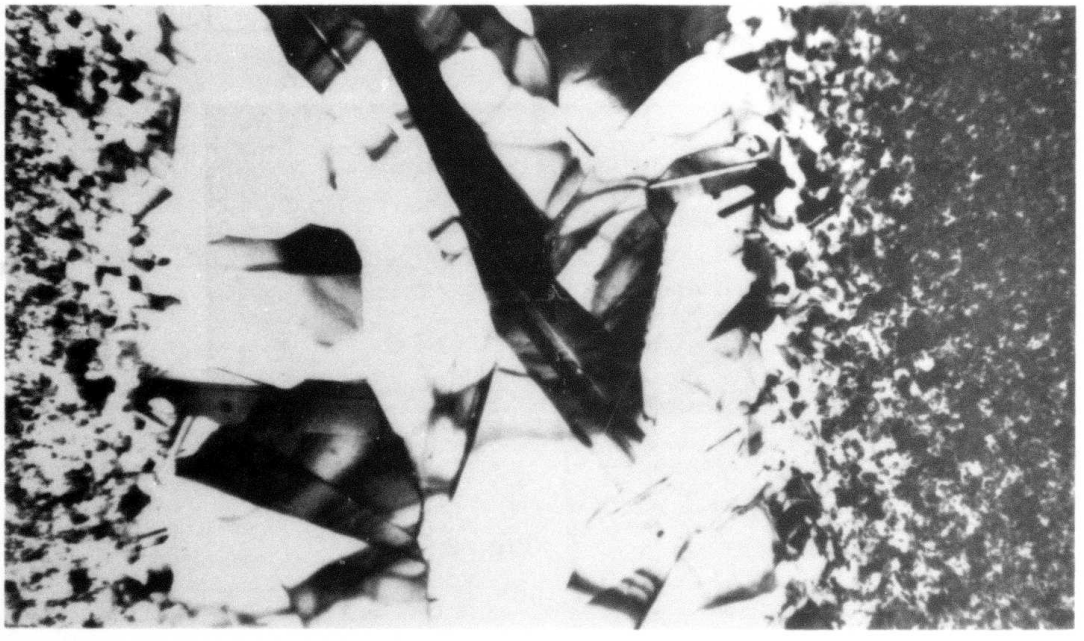


Fig. 2

SINGLE LINE AND OVERLAP EFFECT IN L.A.



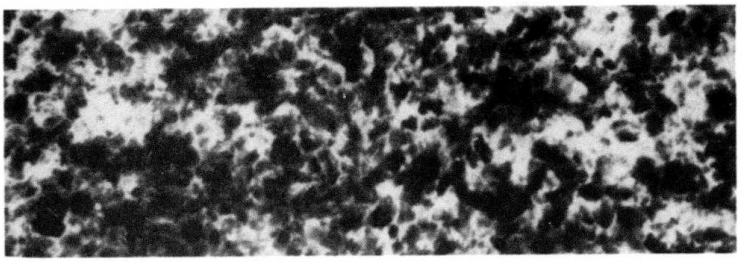
0.3μ 8.5W OVERLAP SCAN



3μ 8.0W SINGLE LINE

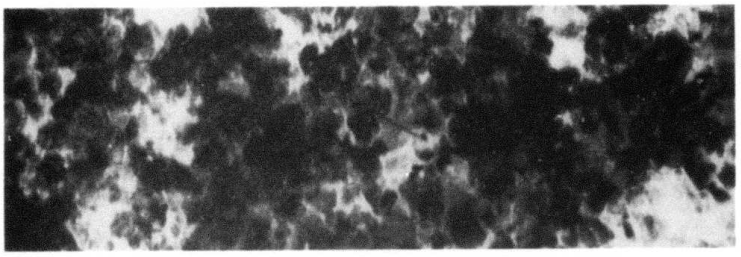
Fig. 3

7W



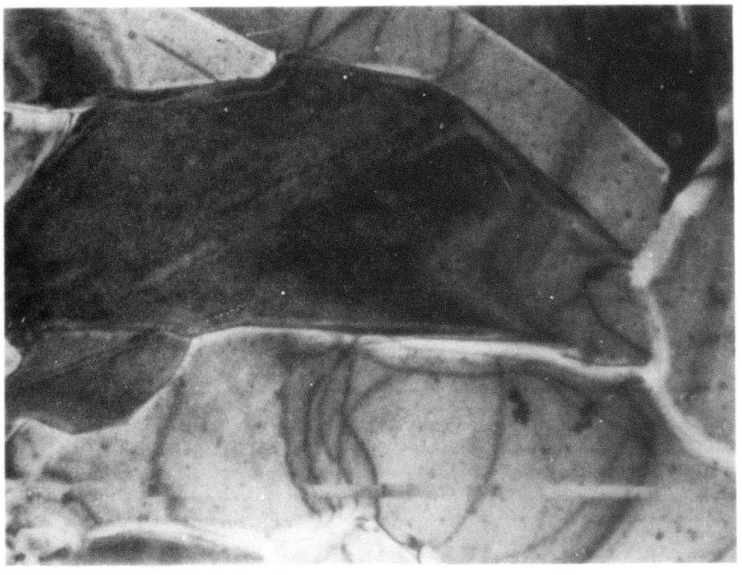
0.5μ

9W



0.5μ

11W



5μ

Fig. 4

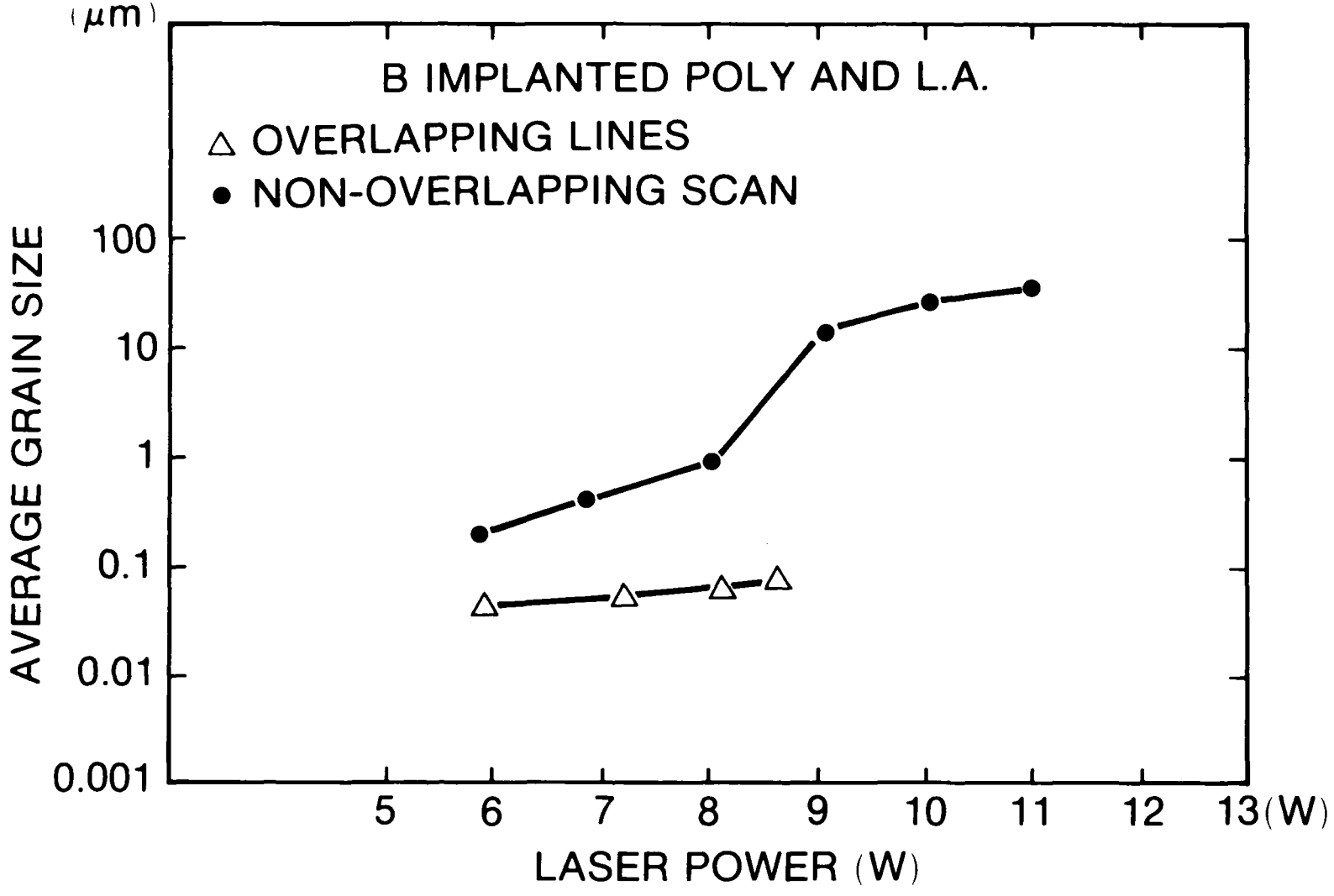

(μm)
B IMPLANTED POLY AND L.A.
△ OVERLAPPING LINES
● NON-OVERLAPPING SCAN
AVERAGE GRAIN SIZE
100
10
1
0.1
0.01
0.001
5
6
7
8
9
10
11
12
13(W)
LASER POWER (W)

Fig. 5

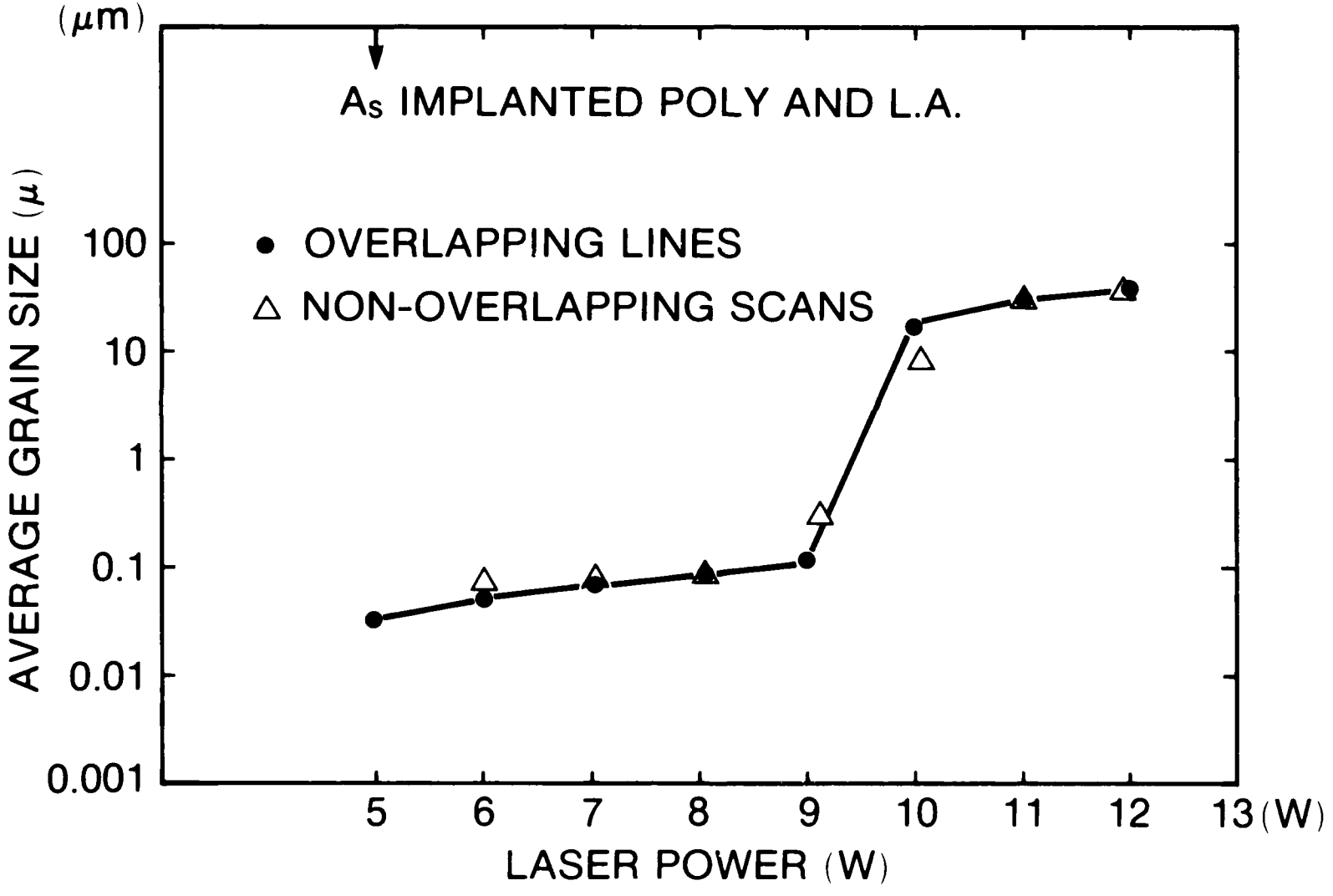

(μm)
As IMPLANTED POLY AND L.A.
AVERAGE GRAIN SIZE (μ)
100
10
1
0.1
0.01
0.001
OVERLAPPING LINES
NON-OVERLAPPING SCANS
5
6
7
8
9
10
11
12
13 (W)
LASER POWER (W)

Fig. 6

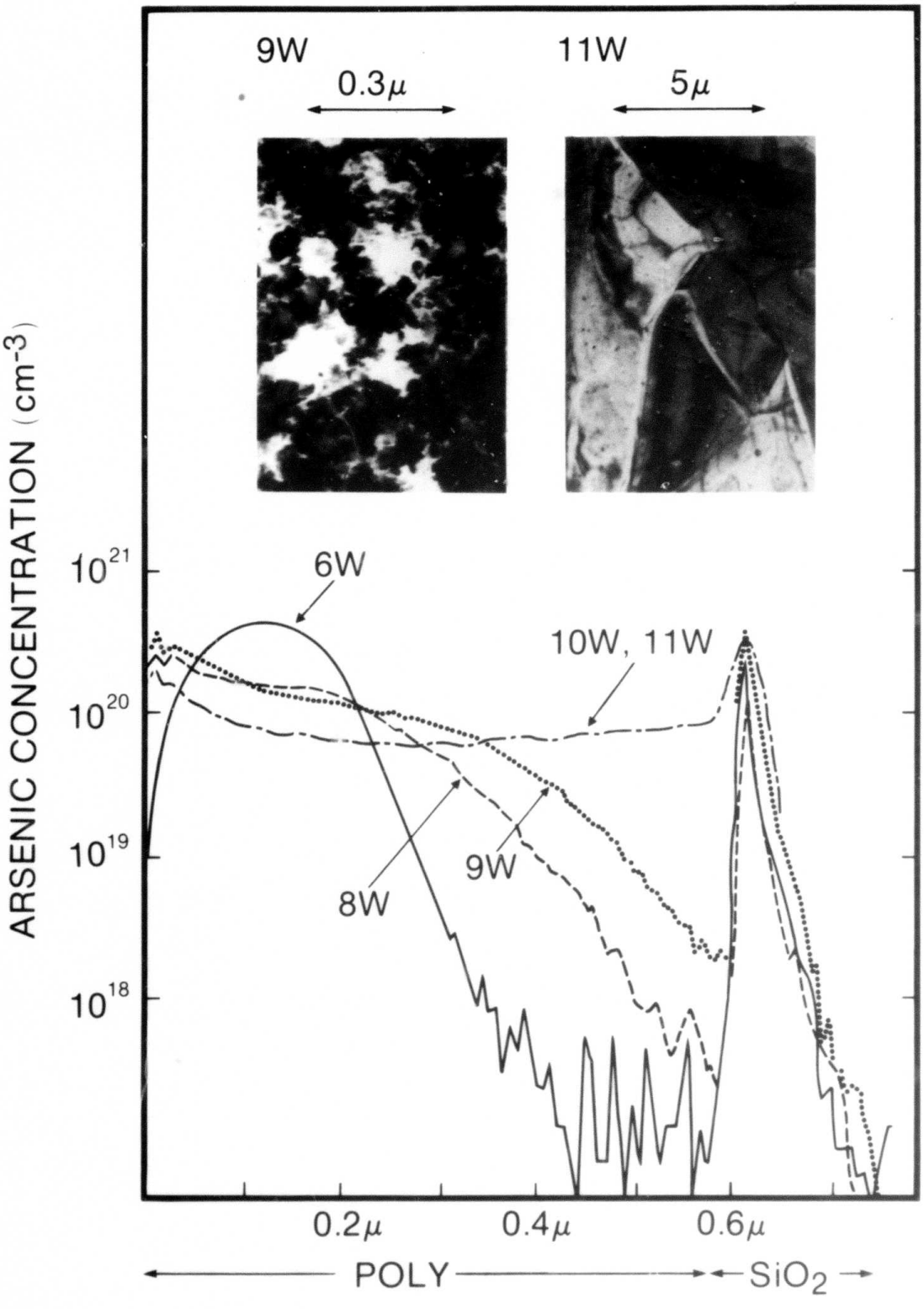

9W
0.3μ
11W
5μ
ARSENIC CONCENTRATION (cm-3)
10^21
10^20
10^19
10^18
6W
10W, 11W
9W
8W
0.2μ
0.4μ
0.6μ
POLY
SiO2

Fig. 7

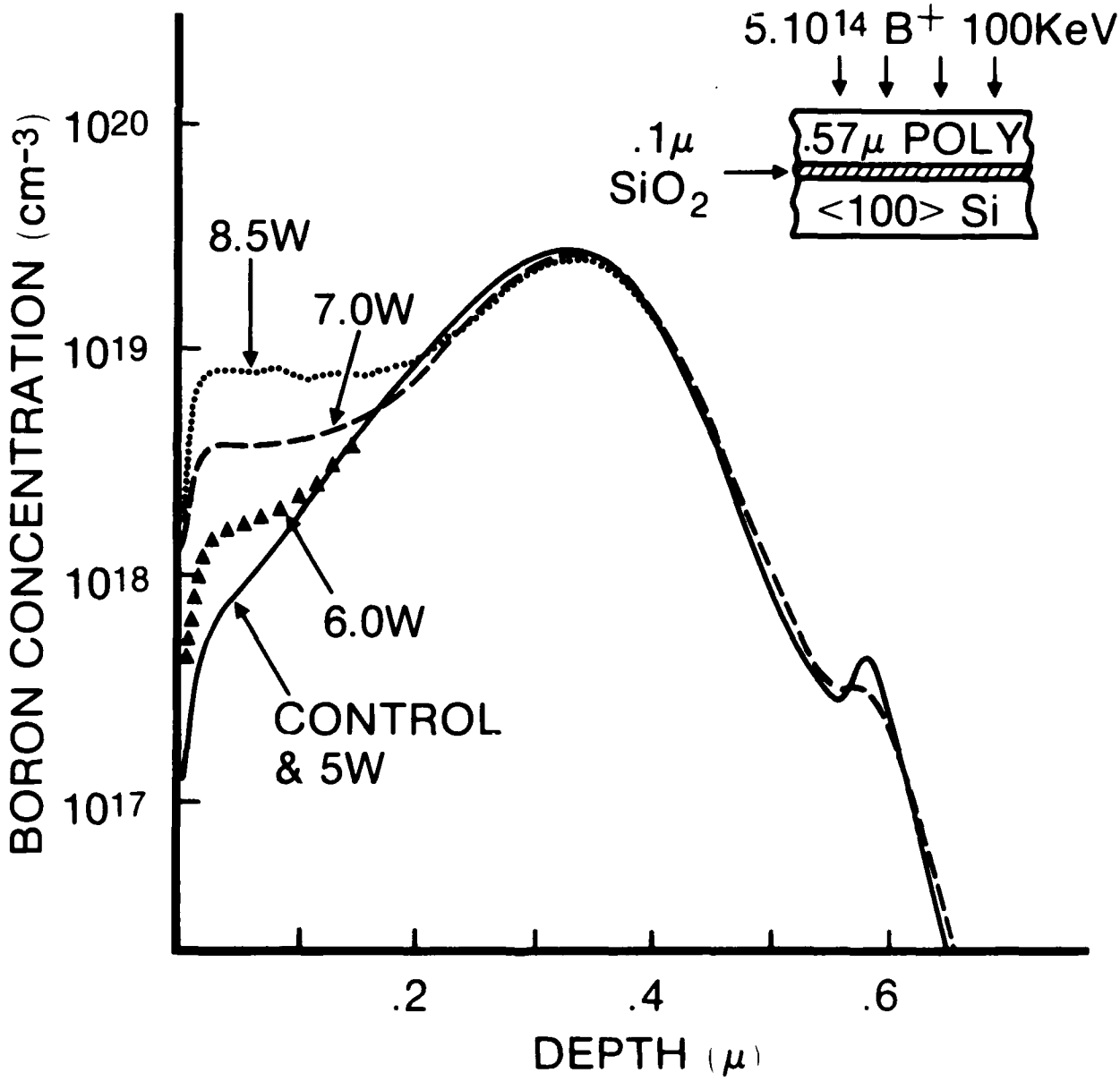

5.10^14 B+ 100KeV
.1μ SiO2
.57μ POLY
<100> Si
8.5W
7.0W
6.0W
CONTROL & 5W
BORON CONCENTRATION (cm-3)
1020
1019
1018
1017
.2
.4
.6
DEPTH (μ)

Fig. 8

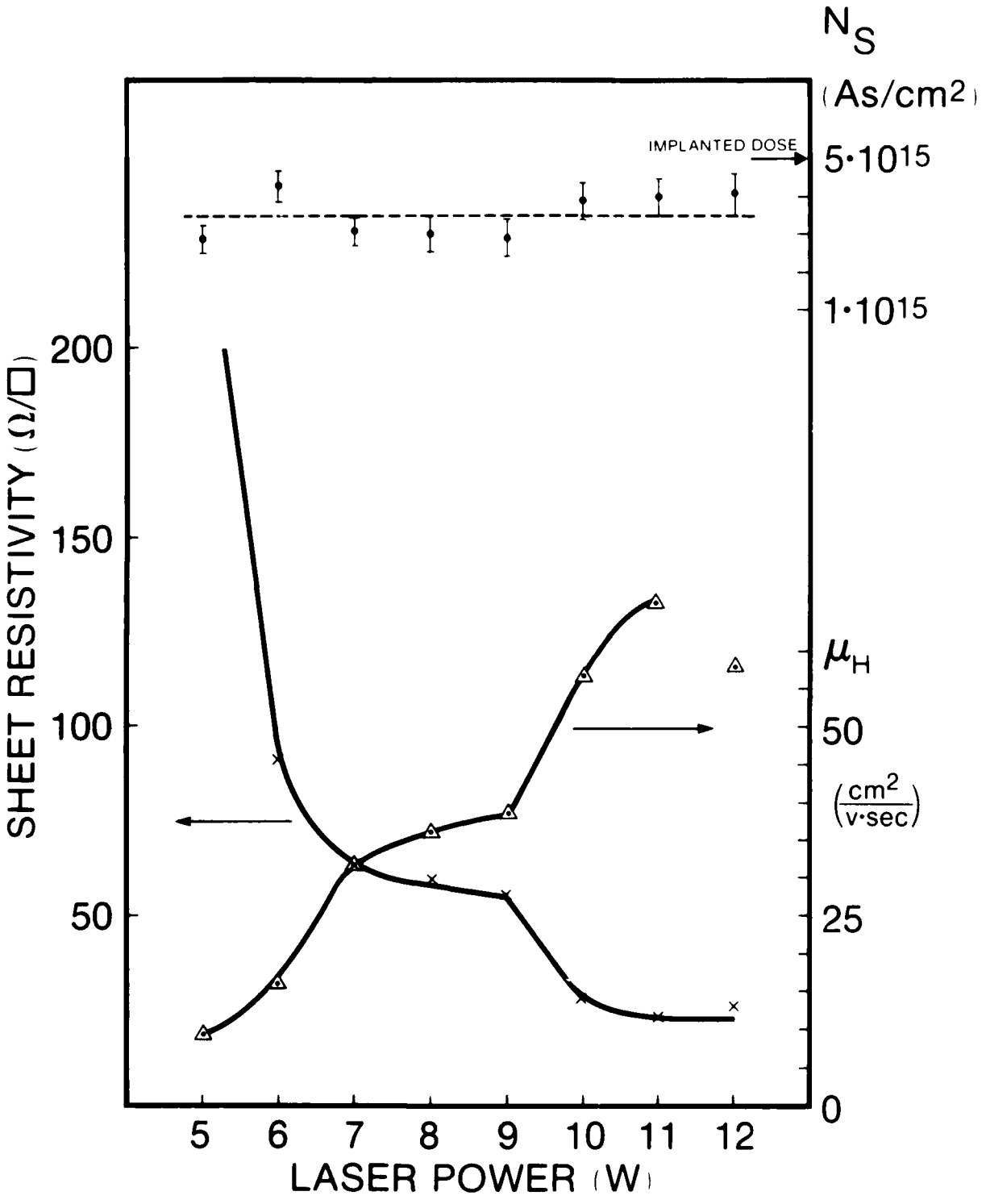

N_S
(As/cm²)
IMPLANTED DOSE
5·10¹⁵
1·10¹⁵
SHEET RESISTIVITY (Ω/□)
200
150
100
50
μ_H
50
25
0
$\left(\frac{cm^2}{v \cdot sec}\right)$
5 6 7 8 9 10 11 12
LASER POWER (W)

Fig. 9

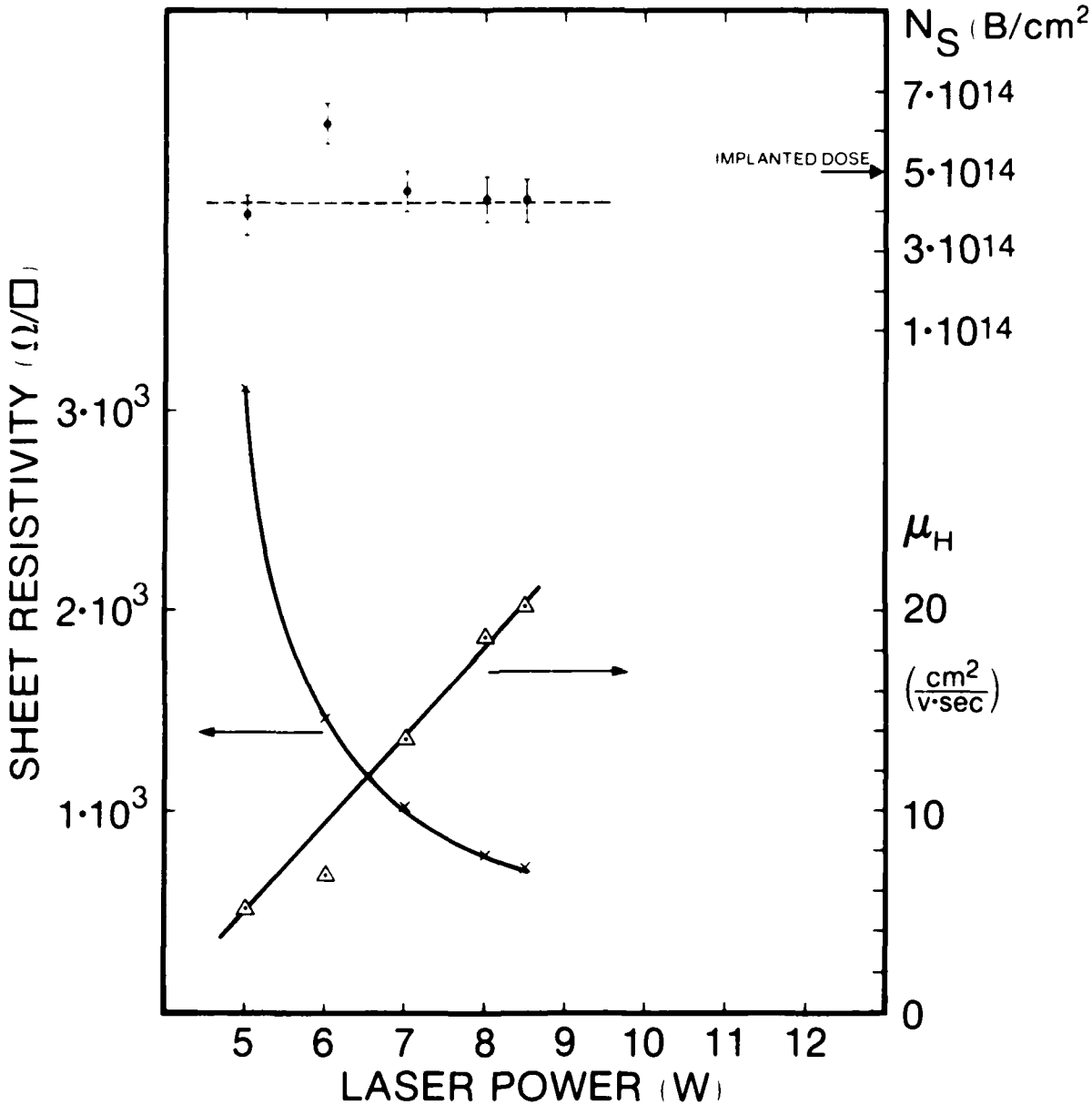

N_S (B/cm^2)
7·10^{14}
IMPLANTED DOSE
5·10^{14}
3·10^{14}
1·10^{14}
SHEET RESISTIVITY (Ω/□)
3·10^3
2·10^3
1·10^3
μ_H
20
$\left(\frac{cm^2}{v \cdot sec}\right)$
10
0
5
6
7
8
9
10
11
12
LASER POWER (W)

Fig. 10

RESISTIVITY REDUCTION IN HEAVILY DOPED POLYCRYSTALLINE SILICON USING CW-LASER AND PULSED LASER ANNEALING

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ABSTRACT

The resistivity reduction in heavily doped polycrystalline Si by laser annealing and its increase during subsequent heat processing have been studied. Both cw and pulsed lasers have been used for the experiments and the results are compared. In both cases laser annealing reduces the Si resistivity by a factor of 2-3 compared to the furnace annealing. A limited resistivity increase is observed in all laser-annealed Si samples during subsequent thermal annealing, with the final values for resistivity being lowest for cw-laser annealed Si. The subsequent annealing behaviour observed for cw and pulsed laser annealed Si is interpreted in terms of the different grain structures found in these films. It is demonstrated by TEM studies that the resistivity instability is caused by the precipitation of dopants in the form of rod shaped structures localized at the grain boundaries as well as within the crystallites.

I INTRODUCTION

Polycrystalline silicon (denoted hereafter by "silicon") is a commonly used material in integrated circuit technology. Since gates and interconnection lines in MOS integrated circuits are usually formed by a thin layer of doped Si, the reduction of its resistivity is a basic requirement for the high speed operation of circuits. Doping of the Si film is usually done by such techniques as in situ incorporation during the deposition, ion implantation or thermal diffusion. The lowest resistivity obtainable, for instance, by $POCl_3$ diffusion at 1000°C, is 450 μΩ-cm. It is very difficult to obtain any additional reduction in resistivity by the conventional methods.

Gat et al. [1] demonstrated that cw-Ar laser annealing can be applied to reduce the sheet resistivity of the doped Si films. They obtained smaller values, by more than a factor of two, for the laser annealed Si compared to that obtained by the thermal annealing. Wu and Magee [2], and Shibata et al. [3], also reported a similar effect using pulsed lasers. However, it was also pointed out that the resistivity reduction by pulsed laser annealing was not thermally stable [3]. It was shown that the resistivity was substantially increased above the initial values during subsequent thermal annealing after the laser anneal. Some examples of this problem are presented in Fig. 1. The samples were heavily phosphorus doped Si films that were annealed with a Q switched Nd:YAG laser, and then subjected to the thermal annealing at 450°C or 1000°C. The observed increase in resistivity can present a serious problem when the laser annealing is introduced in an IC manufacturing process.

The purpose of this paper is to investigate and discuss the mechanism of the sheet resistivity reduction in heavily doped Si by laser annealing

and its thermal stability during the post-laser anneal heat treatments. Special emphasis is placed on the varying behavior of pulsed laser or cw laser-annealed Si films. The minimum resistivity of phosphorus doped Si practically obtainable by laser processing is also discussed.

II EXPERIMENTAL

Si films of 1800 Å thick were deposited in a LP-CVD reactor onto 1000 Å Si_3N_4 films which were deposited on <100> single crystal silicon wafers. Phosphorus ions were implanted at 90 keV to varying dose levels (2×10^{15} to 3×10^{16} cm^{-2}). After the implantation, samples were laser annealed using either a cw laser or a pulsed laser. Some of the samples were subjected to thermal annealing only at 1000°C for 30 min., and subsequently used as controls to compare with laser annealed samples.

It is known from the SIMS analysis [4] that the impurity concentration after laser annealing is uniformly distributed within the film. The doping concentration of the Si after the laser anneal can then be calculated from the implant dose divided by the film thickness. In the present experiments, volume concentrations of 1.1×10^{20} cm^{-3} to 1.7×10^{21} cm^{-3} can be anticipated for the implant doses mentioned above. The highest concentration, 1.7×10^{21} cm^{-3}, is comparable to the typical value which can be obtained by conventional $POCl_3$ diffusion.

The cw-laser annealing was performed with a cw-Ar laser operating in the multi-line mode. The laser output was focussed by a 135 mm lens onto the sample and scanned by the apparatus described in Ref. [1]. Typical parameters used in this experiment were $\sim$ 50 μ spot size, 12.0 cm/sec beam scan speed and 350°C substrate temperature. The laser powers of 11 - 13W were typically used, at which powers long grains were formed in the film

along the beam scan direction. For the pulsed laser annealing, an acoustically Q-switched Nd:YAG laser (1.064μ) was utilized. The typical laser parameters were 10 kHz repetition rate, 200 nsec pulse length and approximately 50 μ spot size after focussing by a 30 mm lens. The substrate was held at room temperature. The wafer was scanned by moving the X-Y stage in order that the entire film was covered by successive overlapping pulses. The laser power was adjusted to yield the lowest resistivity of the film without causing any damage to the film. The optimum power was dependent on the doping conditions and was typically used in the range $1 \sim 1.5$W.

Both laser annealed samples and controls were subjected to isothermal annealing at 1000°C in a flowing N_2 ambient. Sheet resistivity, carrier concentration and Hall mobility were measured by the Van der Pauw method. Transmission electron microscope (TEM) studies were performed to aid in explaining the processes occurring within the film after laser and/or thermal annealing.

III RESULTS

A. Electrical Properties

In this section the electrical properties measured by the Van der Pauw method are presented in detail. For simplicity, the abbreviations, CA, PA and TA will be used for cw laser annealing, pulsed laser annealing and thermal annealing, respectively, in the remainder of the paper.

Figure 2 shows the resistivity changes in the ion-implanted (3×10^{16} P^+ ions/cm^2), laser annealed Si during thermal annealing at 1000°C. Following laser annealing, the cw laser-annealed Si (CA) exhibited a measured resistivity of 14 Ω/□ , and the pulsed laser annealed Si (PA), 17 Ω/□ . In each case, the resistivity is smaller than that of the thermal annealed

control sample (31 Ω/□). However, it can be noted that the resistivity of either CA or PA increases rapidly in the first stage of thermal annealing. The stable resistivity of PA is ∿ 40 Ω/□ , and is much higher than that of TA. On the other hand, CA rises to only ∿ 20 Ω/□ with the thermal treatment, and remains lower than the control sample. The reason for this large variation presents an interesting problem, and can be further investigated by measuring carrier concentration and mobility.

The changes in the sheet carrier concentration during thermal annealing are shown in Fig. 3. The measured carrier concentration after the laser anneal is approximately the same as the implanted ion dose (3×10^{16} cm^{-2}), implying that almost all the impurities in the film were activated by laser irradiation. The reduced activation for CA (2.2×10^{16} cm^{-2}) will be discussed later.

Figure 3 shows that a rapid deactivation of carriers occurs after a very short duration of thermal annealing. The sheet carrier concentration of CA and PA both relax to the value of about $7 \sim 9 \times 10^{15}$ cm^{-2} ($4 \sim 5 \times 10^{20}$ cm^{-3}) which is in the same range as TA. It should be noted that the carrier concentration of CA after the deactivation is larger than that of PA or TA. These differences, however, are not large enough to explain the large variations in sheet resistivity shown in Fig. 2.

Figure 4 shows the Hall mobility as a function of thermal annealing time. It can be seen that the mobility of the laser annealed polycrystalline Si increases rapidly during the first stage of the thermal annealing. This increase can be related to the decrease in the carrier concentration (Fig. 3) leading to a reduction in the number of the charged scattering centers. The mobility of CA after the initial increase is approximately 33 $cm^2/V \cdot sec$ and is close to the single crystal mobility of 38 $cm^2/V \cdot sec$,

calculated from the Irvin curve [5] at the carrier concentration of the film (5×10^{20} cm^{-3}). However, the mobility of PA is 21 $cm^2/V \cdot sec$, which is much lower than that of CA. This substantial difference in mobility explains the varying stable resistivities of CA and PA. It is shown in the next section that the different values of mobility can be attributed to the difference in the CA and PA grain structures after annealing.

In the following, the implant dose dependences of parameters before and after the heat treatment are presented. Thermal annealing, after the laser anneal, was performed at 1000°C in N_2 ambient for fixed periods of 30 min.

Figure 5 shows the sheet resistivity as a function of the phosphorus implant dose. Open circles (o) and open triangles (Δ) represent resistivities of CA and PA, respectively, before thermal annealing. In case of PA, data is shown only for implant doses greater than 10^{16} cm^{-2}. Pulsed laser annealing of the Si with lower implant doses always led to severe etching of the film when the laser power was increased to get the resistivity lower than TA. The cause of such a difference in etching behavior is not known. The resistivities after the thermal annealing are shown by solid circles (●) and solid triangles (▲) for CA and PA, respectively. The figure shows that the cw laser annealing always gives the lowest resistivity compared to pulsed laser annealing or the thermal annealing (only). Thermal instability of CA is observed only at implant doses higher than 7×10^{15} cm^{-2}. The lowest thermally stable resistivity obtained by cw laser annealing is ∿ 20 Ω/□ (∿ 350μΩ-cm), which represents the lowest resistivity that we can practically achieve by cw-laser annealing in an 1800 Å film. In a 0.5 μm film, which is somewhat more typical of IC fabrication, we expect a minimum sheet resistance of approximately 7 Ω/□ .

The implant dose dependence of the sheet carrier concentration and the Hall mobility are given in Fig. 6. The data are shown for the implant dose range $1 \sim 3 \times 10^{16}$ cm^{-2} where the resistivity instability occurs. The symbols used here are the same as those used in Fig. 5. In Fig. 6(a), it is shown that almost all the impurities implanted were activated either by cw or pulsed laser annealing. Only the CA with the highest implant dose (3×10^{16} cm^{-2}) exhibits a noncomplete activation. The deactivation of impurities after the subsequent thermal annealing is, however, observed for all laser annealed samples examined here. It is seen from the figure that the maximum concentration of the thermally stable activated impurity is approximately 9×10^{15} cm^{-2} (5×10^{20} cm^{-3}), and is achieved by the cw laser annealing. The implant dose dependence of Hall mobility is shown in Fig. 6(b). The increase in mobility after the thermal annealing is most probably associated with the deactivation of impurities which decreases the number of charged scattering centers. Quantitative analysis of mobility is given in the discussion section.

From the electrical measurements presented above, we can summarize the results as follows: the sheet resistivity reduction in doped Si films by laser annealing is achieved by two separate processes; one is the (nearly) complete activation of impurities and the other is the mobility increase due to the grain growth by the laser. However, the activation of impurities in excess of a solid solubility is not thermally stable, and only the resistivity reduction due to the increase in mobility survives after the subsequent thermal annealing. It is shown in the next section that the cw-laser annealing can form long grains in the Si film, while the pulsed laser annealing produces a complicated grain structure with no substantial grain growth. That leads to a larger mobility for CA, namely the lowest

resistivity which is thermally stable. It was suggested in Ref. 3 that the deactivation of carriers happens via precipitation of dopants within the grain crystallites and also at the grain boundaries. If this is true, the largest stable carrier concentration for CA can be easily understood, because the small grain structures found in PA and TA provide larger areas of the grain boundary which serve as sinks for impurity atoms. This postulate has been carefully examined by transmission electron microscopy, and the results are presented in Section III-B.

B. Transmission Electron Microscopy

Conventional jet thinning techniques were used to prepare samples for TEM analysis as described in an earlier publication [1]. Control TA, PA, and CA samples ion implanted to various dose levels were examined and the data compared to results obtained from laser annealed samples subjected to subsequent thermal anneal treatments.

In Fig. 7 we show representative bright field electron micrographs obtained on as-deposited and ion implanted ($3 \times 10^{16}/cm^2$) TA, PA, and CA samples. The as-deposited film [Fig. 7(a)] exhibits a fine grained polycrystalline structure with average grain size, $\sim$ 500 Å. After implantation and annealing at 1000°C for 30 min., the average grain size increased to $\sim$ 0.3 μm, as shown in Fig. 7(b). In contrast, PA exhibited a relatively non-uniform pattern of grain growth, characterized by the presence of annular zones of grain enlargement surrounded by a matrix of smaller grains [Fig. 7(c)]. In all cases, there was no significant differences in the sizes of grains observed within the annular grain enlargement regions and the average grain size of TA. The CA [Fig. 7(d)] exhibited grains of average dimensions, 2 μm x 20 μm, arranged in a chevron pattern

along the laser scan direction. Selected area diffraction patterns obtained through the entire film thickness and from sectioned samples show that the grains are single crystal columnar structures extending from the nitride layer to the surface of the film with no evidence of an identifiable preferred orientation.

Of particular interest for the PA and CA [Figs. 7(c) and 7(d)] is the fact that there is no evidence of precipitation at either the grain boundaries or within individual grains immediately after laser annealing. For samples implanted to dose levels less than $10^{16}/cm^2$, TA, PA, and CA poly also exhibited no clear indication of precipitation or dopant segregation at grain boundaries. In addition, after subsequent thermal anneals at 1000°C, these films showed no additional evidence of second phase structures appearing within the grains or at the grain boundaries. The results suggest that precipitation is either absent or the density of precipitates sufficiently low so as to escape detection by TEM.

In comparison, for higher dose levels of $3 \times 10^{16}/cm^2$, we obtained evidence of precipitation at the grain boundaries of both CA and PA subjected to a 1000°C thermal anneal. However, the detection of precipitates by diffraction contrast techniques is severely restricted in fine grained poly structures. The superposition of strain fields from adjacent grain boundary regions will necessitate either a large precipitate or a sufficiently large precipitate strain field to render the segregation region "visible" above background intensity levels in most fine grained poly samples. In comparison, precipitation within CA is more easily detected because of extremely large grain sizes and adequate separation of adjacent boundary regions, thereby yielding a relative relaxation in visibility/contrast criteria.

In Fig. 8(a), we show a representative bright field electron micrograph of a sample implanted to a dose level of $3 \times 10^{16}/cm^2$, followed by a CA + 1000°C thermal anneal. We observe the presence of rod shaped precipitates ~ 1000 Å to 5000 Å in length within the interior of individual grains. These linear precipitates were observed repeatedly in CA samples subjected to subsequent thermal anneals. To further investigate the spatial distribution of the rod-shaped structures, we immersed another set of samples in HF acid (undiluted) for approximately 30 minutes. After cleaning, the structures were then jet thinned from the back of the wafer and the Si layer examined in the electron microscope. In Fig. 8(b), we observe that immersion in the HF acid solution left the Si intact but selectively etched the precipitate regions (white lines) to reveal their positioning within the interior of the grain and at the grain boundaries. It is interesting to note that the precipitate density at the grain boundaries greatly exceeds the rod density within the individual grains, implying that a substantial fraction of the segregated impurity concentration is localized at the grain boundaries.

To obtain additional comparative data, samples implanted to a dose level of $3 \times 10^{16}/cm^2$ were also exposed to the etch solution immediately after laser annealing (no thermal anneal) and subsequently prepared for TEM analysis. The results showed no evidence of selected etch features or precipitates occurring in any of the samples examined, confirming that precipitation occurs only after thermal treatment of the laser annealed poly.

From the data obtained in these experiments, we can conclude from direct TEM observation that thermal annealing at 1000°C after pulsed or cw laser annealing of phosphorus ion implanted ($> 10^{16}/cm^2$) samples produces

clear evidence of impurity precipitation in the form of rod shaped structures localized within grains and at the grain boundaries.

IV. DISCUSSION

We have demonstrated that the sheet resistivity changes in Si films by laser annealing and subsequent thermal annealing can be satisfactorily interpreted in terms of changes in crystallographic structure of the film and activation/deactivation of dopants.

The dramatic decrease in sheet resistivity by laser annealing is achieved by a nearly 100% activation of implanted impurities. The highest carrier concentration (which is also equal to the number of activated impurities) achieved by the laser is more than 10^{21} cm^{-3} which exceeds the solid solubility limit of phosphorous ($\sim 4 \times 10^{20}$ cm^{-3} [6]) in single crystal silicon.

The activated impurities in excess of the solid solubility are, of course, thermally unstable, resulting in the formation of precipitates during subsequent heat treatments. Precipitation occurs at the grain boundaries as well as in the grain crystallites. Precipitation has been verified through the TEM studies in Section III-B. The grain boundary precipitation explains why the carrier concentration of PA after the thermal annealing (Fig. 3) is the smallest, since the fine grain structure found in PA provides a largest area of grain boundary.

The incomplete activation of implanted impurities found in CA at the highest dose of 3×10^{16} cm^{-2} [Fig. 6(a)] can be understood by the precipitation of impurity occuring during the laser scan. In cw laser annealing, each of the line scans are overlapped to cover a large area. During each single scan the adjacent, already laser-annealed region is

subjected to a lower temperature laser anneal due to the Gaussian-like temperature distribution produced by the laser beam. We believe this short time (of the order of beam dwell time, $\sim$ msec) is nonetheless sufficient to cause precipitation to occur. This has been verified by performing cw laser annealing on a sample in which impurities were fully activated to about 3×10^{16} cm^{-2} by a pulsed laser anneal. The cw-laser scan with a lower power of 9W reduced the carrier concentration to 1.6×10^{16} cm^{-2}.

The varying values of mobility shown in Figs. 4 and 6(b) can be attributed to the differences in the average grain size of the Si film. It is instructive to replot the data of Fig. 6(b) in such a manner that mobility is shown as a function of active impurity concentration. The results are given in Fig. 9. The symbols used are the same as in Figs. 5-6, where the solid line indicates the mobility calculated from the Irvin curve assuming 100% activation of dopants. It is seen that the mobility of CA is nearly equal to the single crystal mobility (Irvin mobility) within the experimental error, while that of PA or TA is fairly small.

The dotted lines in Fig. 9 represent the calculated mobility of heavily doped Si with the grain size as a parameter. The previous theoretical calculations on Si resistivity [7,8] cannot be applied to the heavily doped Si discussed here. Recently, a detailed calculation which can be used at this high doping concentration range was developed [9]. However, we used a simplified model here. We assume that the electrical conduction through the grain boundary is given by the thermionic emission current,

$$Jth = qn \left(\frac{kT}{2m^*}\right)^{1/2} \exp\left(-\frac{qV_B}{kT}\right) \left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \qquad (1)$$

where V_a is the applied voltage, q is the electronic charge, n is the carrier density, m^* is the electronic effective mass and V_B is the potential barrier

height at the grain boundary. For small applied voltage, $qV_a \ll kT$, Eq. (1) reduces to

$$Jth = \frac{1}{r_g} V_a \tag{2}$$

where

$$r_g^{-1} = q^2 n \left(\frac{1}{2m^*\pi kT}\right)^{1/2} \exp - \frac{qV_B}{kT} \quad q.n\alpha \tag{3}$$

which gives the effective grain boundary resistance, r_g (Ω/cm^2). The carriers near the grain boundary are trapped by the trap states existing at the boundary, leading to a depletion layer. This depletion layer width was calculated for the most lightly doped sample ($\sim 1 \times 10^{15}$ cm^{-2}, or $\sim 5 \times 10^{19}$ cm^{-3}) assuming the trap density of 3×10^{12} cm^{-2} given in Ref. [7]. The depletion width obtained was 6 Å, which is much smaller than the typical grain size (0.5 μ ~ 20μ) and can be neglected for doping concentrations which we are concerned with here ($> 5 \times 10^{19}$ cm^{-3}). Thus the Si with average grain size of L (cm) can be approximated as a chain of uniformly doped single crystals of size L which are separated from each other by infinitesimally thin resistive sheets. As a result the effective resistivity of Si can be written as,

$$\rho_{eff} = (r_g + \rho \cdot L)/L$$

where ρ is the resistivity of a single crystal. The effective mobility of the Si is given by

$$\frac{1}{\mu_{eff}} = \frac{1}{L\alpha} + \frac{1}{\mu_o} \tag{4}$$

where μ_o is the Irvin mobility and α is defined in Eq. (3). α can, in principle, be calculated if we know the potential barrier height V_B. Here, we experimentally determined the value of α as a function of doping

concentration by fitting Eq. (4) to the data of TA in Fig. 10, where we used the average grain size (L = 3300 Å) determined from the TEM measurements.

The calculated results for L = 1μ, 5μ and 10μ are shown in Fig. 10 by dotted lines. It is easily seen that the mobility of sheet Si is essentially the same as the Irvin mobility when the grain size is larger than 5μ. This is approximately the case for CA which has long grains with a typical size of 2μ x 20μ.

The apparently different behavior of cw or pulsed laser annealed Si can be simply attributed to the different grain structures of these films shown by the TEM pictures (Fig. 7). The formation of different grain structure by cw-laser or pulsed laser anneal can be explained by the difference in the cooling rates. It should be remembered that the laser powers used in the experiments were high enough to melt the Si in either case.

In the case of a cw-laser, the laser beam is scanned across the wafer with a constant scan speed (12 cm/sec). The molten region in the Si film moves with the scanned beam and solid-liquid interface advances with the same speed with the beam. This situation is analogous to that in floating zone crystal growth and allows long grains to form along the beam scan direction.

However, the situation is totally different in the case of a pulsed laser. The annealing is performed by successive overlapping of laser pulses. The cooling rate produced by a pulsed laser is very large ($\sim 10^{10}$ degree/sec) and the crystal growth is governed by a heterogeneous nucleation from a super-cooled melt, which explains the fine grain matrix of PA shown in Fig. 8.

The occurrence of relatively larger grains ($\sim$ 1 μm) in an angular pattern is also shown in the same figure, which can be explained qualitatively with reference to Fig. 10. A single laser shot produces a Gaussian-like temperature distribution in the film. In the region where the temperature is higher than

the Si melting temperature, the material passes to the liquid phase. Grain growth within the liquid region can then occur only after sufficient cooling to reduce the temperature below the melting temperature.

A qualitative sketch of the time changes in the temperature profile is given in Fig. 10, where t_0, t_1 and t_2 are assumed to be a time sequence with the same time intervals. The intersection of the temperature profile with the melting temperature line thus moves toward the center of the beam (A → C) during the cooling. The speed for this point to move can be expected to be very large when it approaches the center (B → C). Here the heterogeneous nucleation occurs, leading to a fine grain structure. However, the speed is presumably slow enough in the beginning of cooling (A → B) for homogenous nucleation to occur, which allows relatively large grains ($\sim$ 1 μ) to form in a radial direction, possibly nucleating on adjacent grains in the unmelted region outside A. Successive overlapping pulses would then form overlapping rings of relatively large grains surrounding areas of fine grains. This can account for the occurrence of the peculiar grain structure found in PA films.

However, it should be noted that this discussion holds only for the case where each laser pulse melts the whole irradiated area. If the laser power is carefully adjusted to melt only the fine grain region without melting the already recrystallized region, we may also get a large grain structure by overlapping pulsed laser beams.

V. CONCLUSIONS

The resistivity reduction in heavily doped Si by laser annealing and its increase during subsequent thermal annealing have been studied. Although both cw and pulsed lasers were used for the experiments, the quantity of primary

importance is not the type of the laser used but the grain structure of Si produced by the laser.

In the resistivity reduction of Si film by laser annealing, two separate processes are involved: the increase of carrier mobility by forming large grains and the increase of carrier concentration through (nearly) 100% activation of dopants. The mobility increase due to grain growth is thermally stable, while the activation of dopants over the solid solubility is not thermally stable, leading to the deactivation of dopants during the subsequent thermal process. The TEM studies showed that the deactivation occurs by forming rod-shaped precipitates at the grain boundaries as well as within the grain crystallites. The cw laser can form large grains ($\sim 2\mu \times 20\mu$), which increases the mobility of heavily doped Si up to almost a single crystal value. However, the pulsed laser annealing produces a complicated grain structure including the very fine grains, which reduces the mobility, and further provides increased area of grain boundaries that act as sinks for dopants. We believe this accounts for the fact that the pulsed laser annealed Si exhibits the highest resistivity after thermal annealing.

Finally, we conclude that the lowest, thermally stable resistivity of the phosphorus doped Si that we can achieve by laser annealing is the single crystal resistivity at a doping level of $\sim 5 \times 10^{20}$ cm^{-3}.

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FIGURE CAPTIONS

Fig. 1 Examples which illustrate the thermal instability occurring in resistivity of pulsed-laser annealed Si. The resistivity of laser-annealed Si (O) and non-laser annealed Si (●) are given as a function of thermal annealing time. The thermal annealing temperatures are: (a) 450°C, (b) 1000°C [Fig. 1(a) was taken from Ref. 3].

Fig. 2 Sheet resistivity of cw-laser-annealed (O) and pulsed laser-annealed (●) Si as a function of thermal annealing time. The samples are 1800Å Si, 3×10^{16} cm^{-2} P^+ implanted with 90 keV. The thermal annealed controls (X) are also shown. The thermal annealing was performed at 1000°C in N_2 ambient.

Fig. 3 Sheet carrier concentration as a function thermal annealing time. The data were taken from the same samples shown in Fig. 2. The symbols used are also the same as appear in Fig. 2.

Fig. 4 Hall mobility as a function of thermal annealing time. The samples and the symbols are the same as in Fig. 2.

Fig. 5 Sheet resistivity of cw laser-annealed Si (O,●) and pulsed laser-annealed Si (Δ,▲) as a function of implant dose. Open symbols (O,Δ) refer to the values following the laser annealing, and solid symbols (●,▲) to the value after the subsequent thermal annealing (30 min, 1000°C). The samples are 1800Å Si films, P^+-implanted at 90 keV. The data for thermal anneal only controls are also shown in the figure.

Fig. 6 Sheet carrier concentration (a), and Hall mobility (b) as a funtion of implant dose. The samples and symbols are the same as in Fig. 5.

Fig. 7 Transmission electron micrographs of 1800Å Si deposited on nitride: (a) as-deposited; (b) thermal annealed only (30 min, 1000°C); (c) pulsed laser-annealed; and (d) cw laser-annealed.

Fig. 8 Transmission electron micrographs of Si subjected to cw laser anneal + 1000°C thermal anneal. a) after laser + thermal anneals; b) after HF etch.

Fig. 9 Hall mobility of Si films plotted as a function of sheet carrier concentration (cm^{-2}) and volume carrier concentration (cm^{-3}). Open (O,Δ) and solid (●,▲) symbols refer to the values before and after the subsequent thermal anneal, respectively. The solid line represents single crystal mobility calculated from the Irvin curve. Calculated mobilities of Si for a variety of grain sizes are also shown by dotted lines.

Fig. 10 Schematical explanation for the grain structure produced by pulsed laser annealing. The upper part of the figure shows the temperature distribution at consecutive sequences, t_0, t_1 and t_2 (the time intervals are assumed to be equal). The intersect of the melting temperature line and the temperature distribution is the solid-liquid interface. Larger grains are formed in region A → B, where the interface movement is slow enough, while fine grains appear in region B → C where the movement is rapid.

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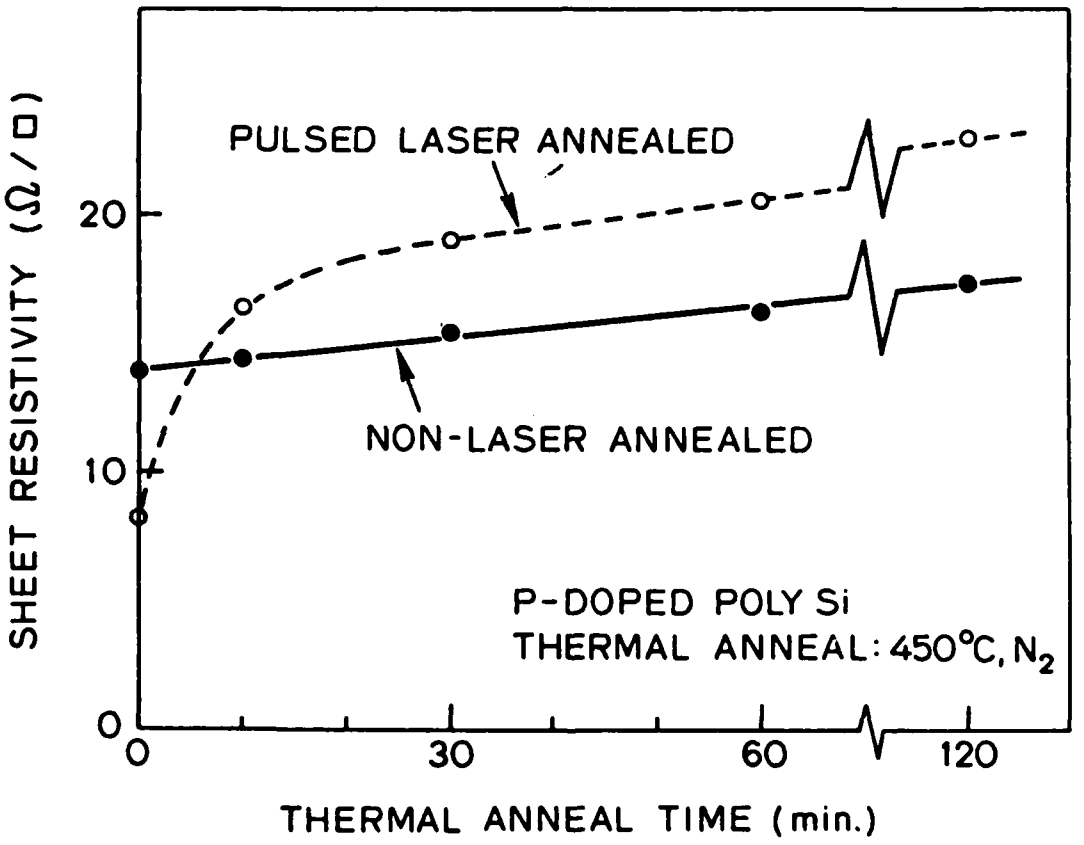

PULSED LASER ANNEALED
NON-LASER ANNEALED
P-DOPED POLY Si
THERMAL ANNEAL: 450°C, N2
SHEET RESISTIVITY (Ω/□)
20
10
0
0
30
60
120
THERMAL ANNEAL TIME (min.)

Fig. 1

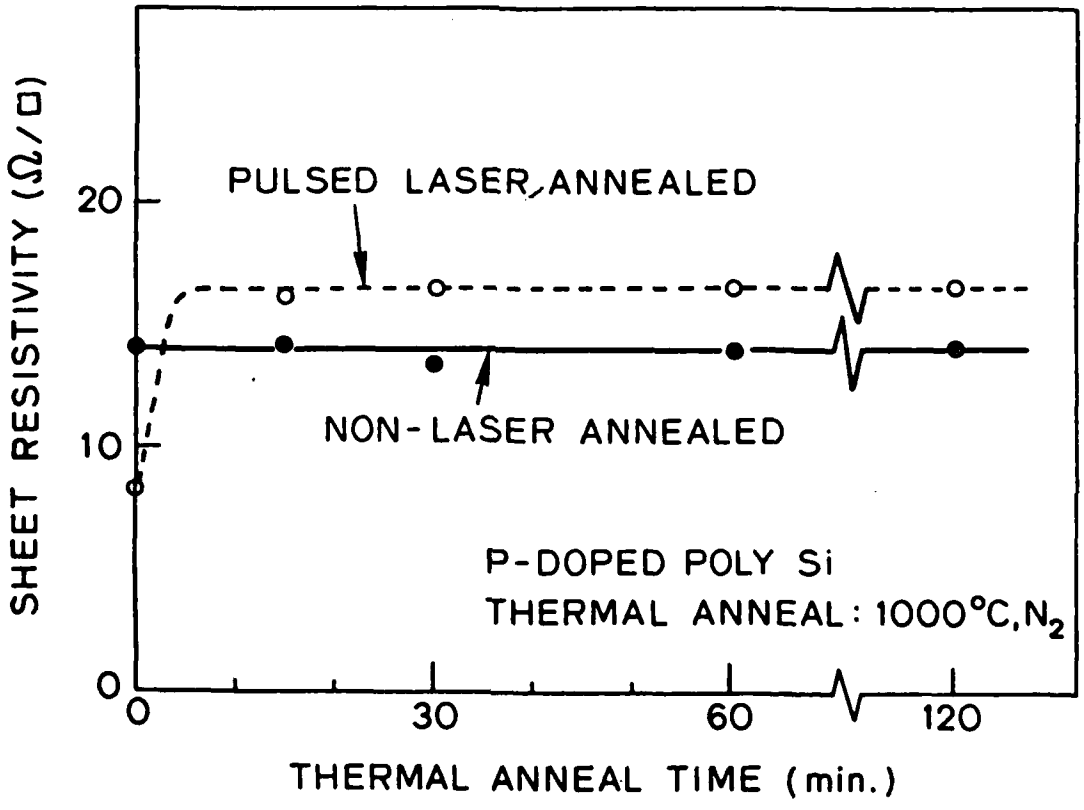

SHEET RESISTIVITY (Ω/□)
20
10
0
PULSED LASER ANNEALED
NON-LASER ANNEALED
P-DOPED POLY Si
THERMAL ANNEAL: 1000°C, N_2
0
30
60
120
THERMAL ANNEAL TIME (min.)

Fig. 2

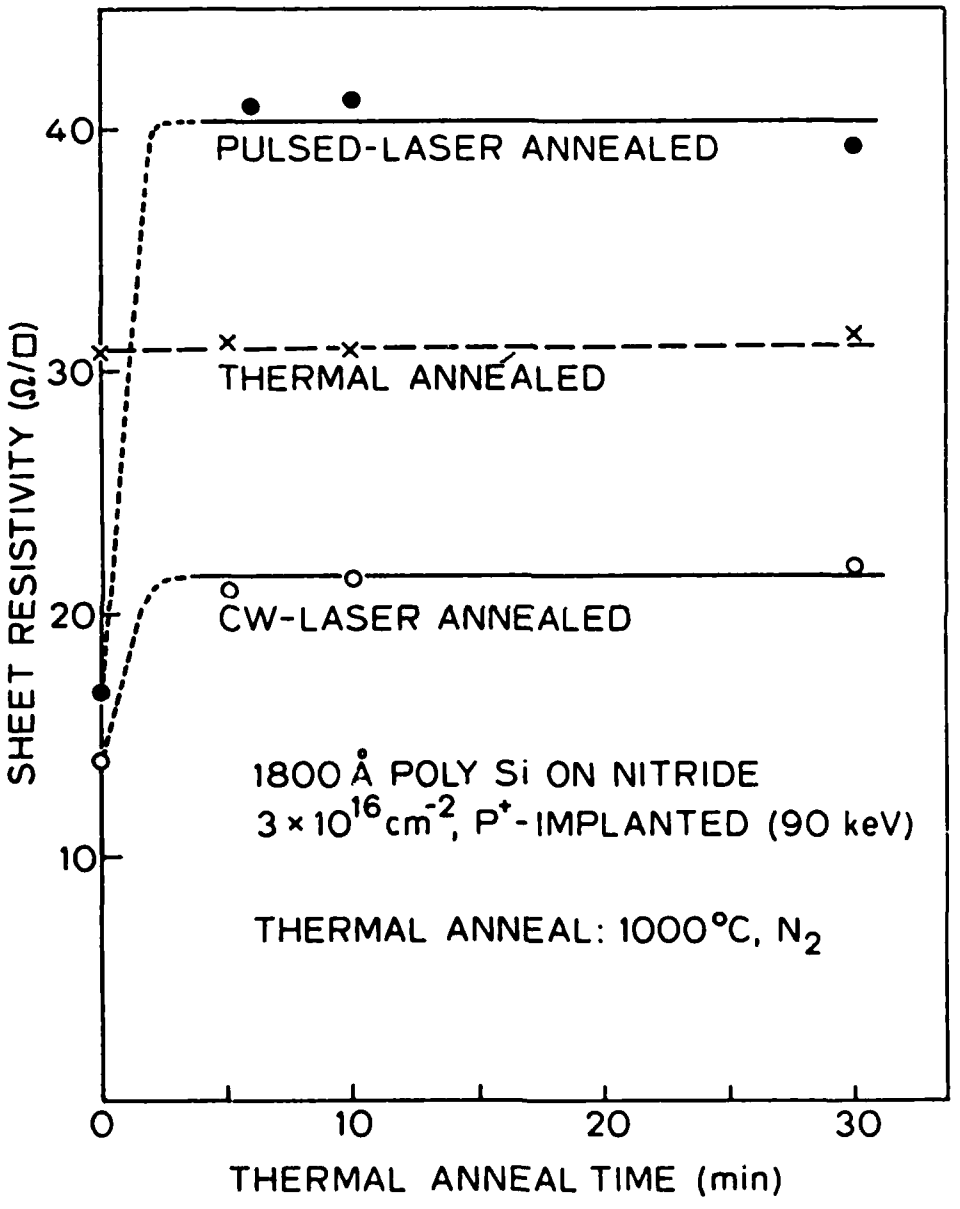

SHEET RESISTIVITY (Ω/□)
40
30
20
10
PULSED-LASER ANNEALED
THERMAL ANNEALED
CW-LASER ANNEALED
1800 Å POLY Si ON NITRIDE
3 × 10^16 cm^-2, P+-IMPLANTED (90 keV)
THERMAL ANNEAL: 1000°C, N2
0
10
20
30
THERMAL ANNEAL TIME (min)

Fig. 3

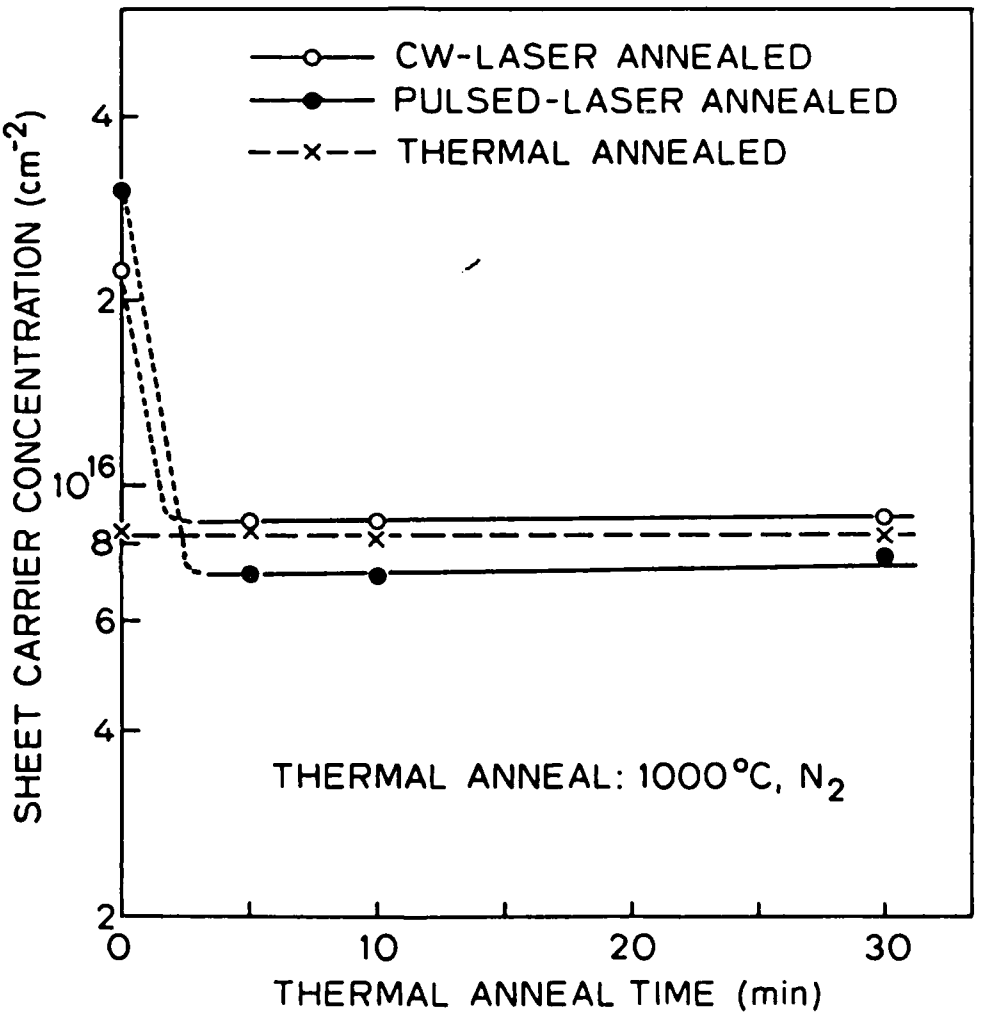

CW-LASER ANNEALED
PULSED-LASER ANNEALED
THERMAL ANNEALED
SHEET CARRIER CONCENTRATION (cm^{-2})
4
2
10^{16}
8
6
4
2
THERMAL ANNEAL: 1000°C, N_2
0
10
20
30
THERMAL ANNEAL TIME (min)

Fig. 4

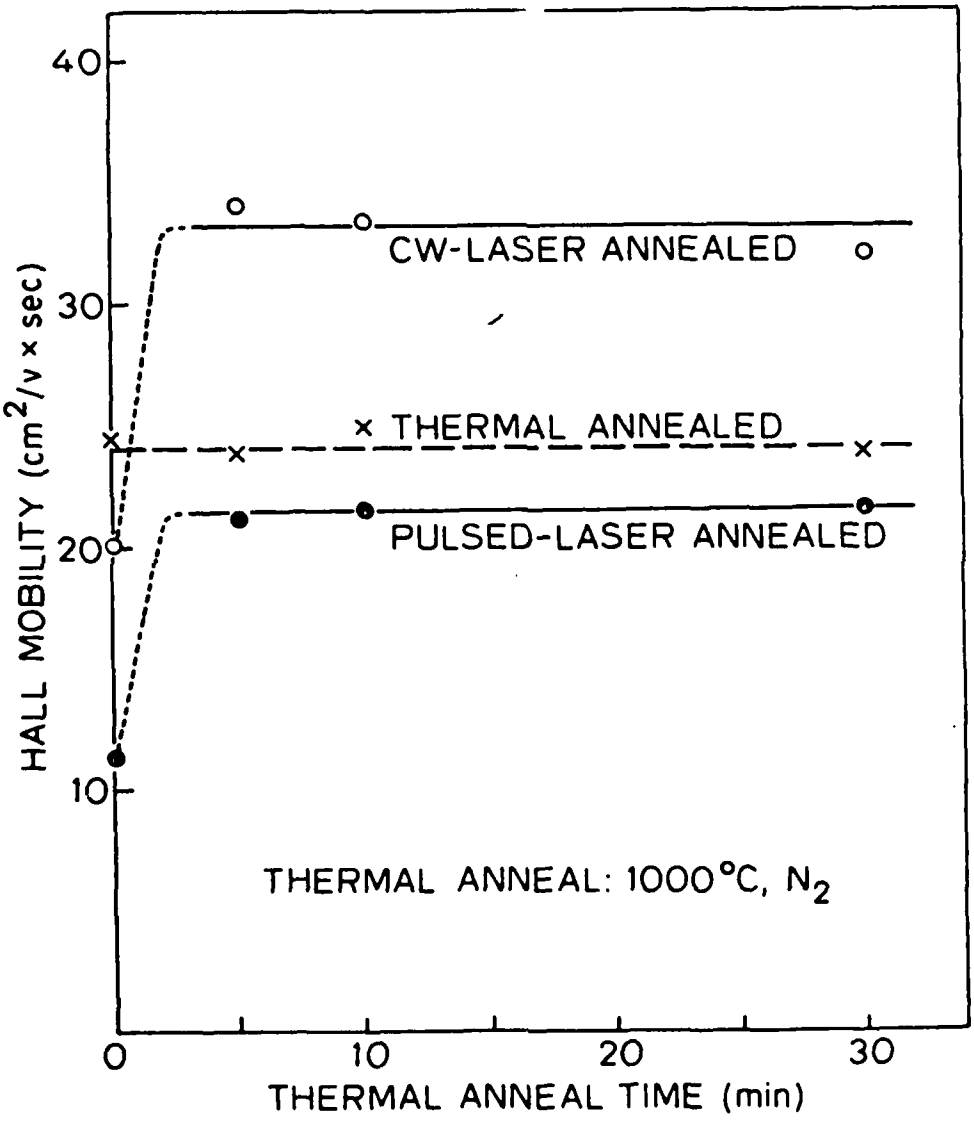

40
30
20
10
HALL MOBILITY (cm²/v x sec)
CW-LASER ANNEALED
THERMAL ANNEALED
PULSED-LASER ANNEALED
THERMAL ANNEAL: 1000°C, N2
0
10
20
30
THERMAL ANNEAL TIME (min)

Fig. 5

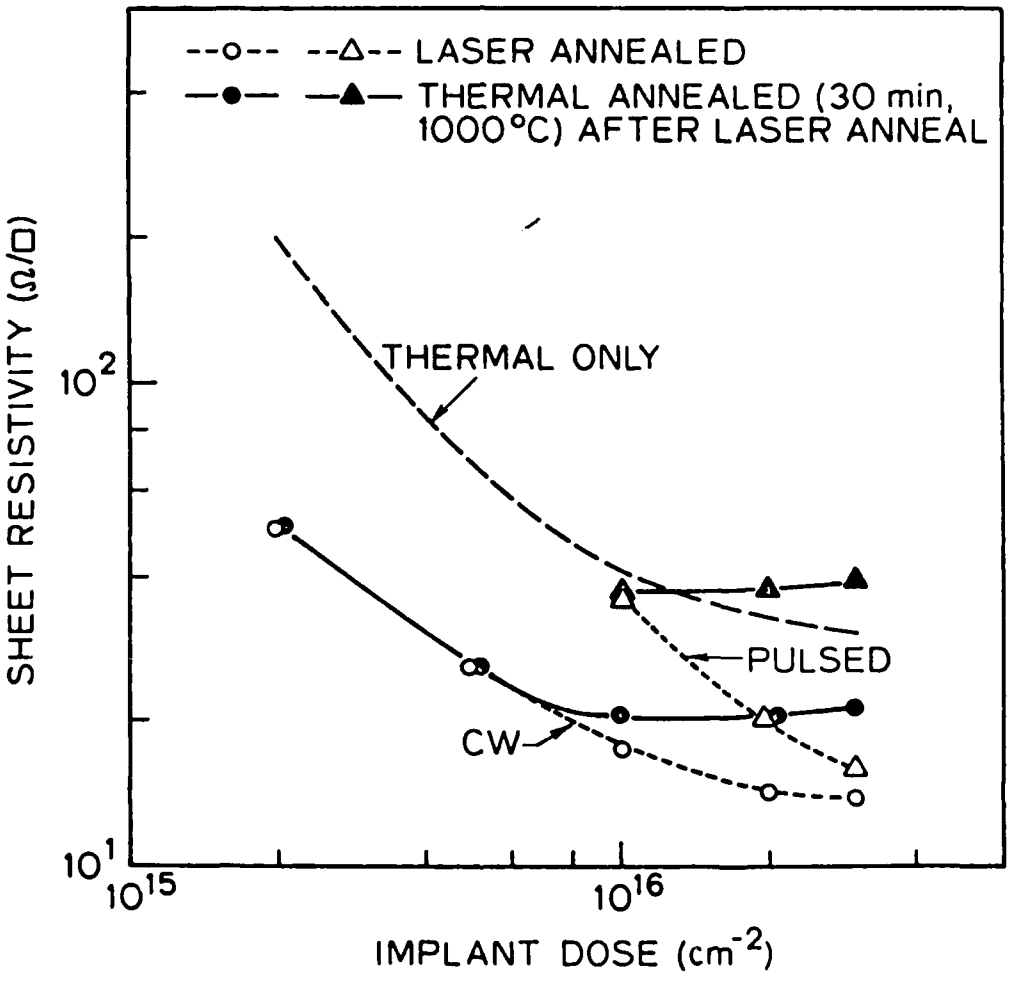

--o-- --Δ-- LASER ANNEALED
—●— —▲— THERMAL ANNEALED (30 min, 1000°C) AFTER LASER ANNEAL
SHEET RESISTIVITY (Ω/□)
10^2
10^1
THERMAL ONLY
PULSED
CW
10^{15}
10^{16}
IMPLANT DOSE (cm^{-2})

Fig. 6

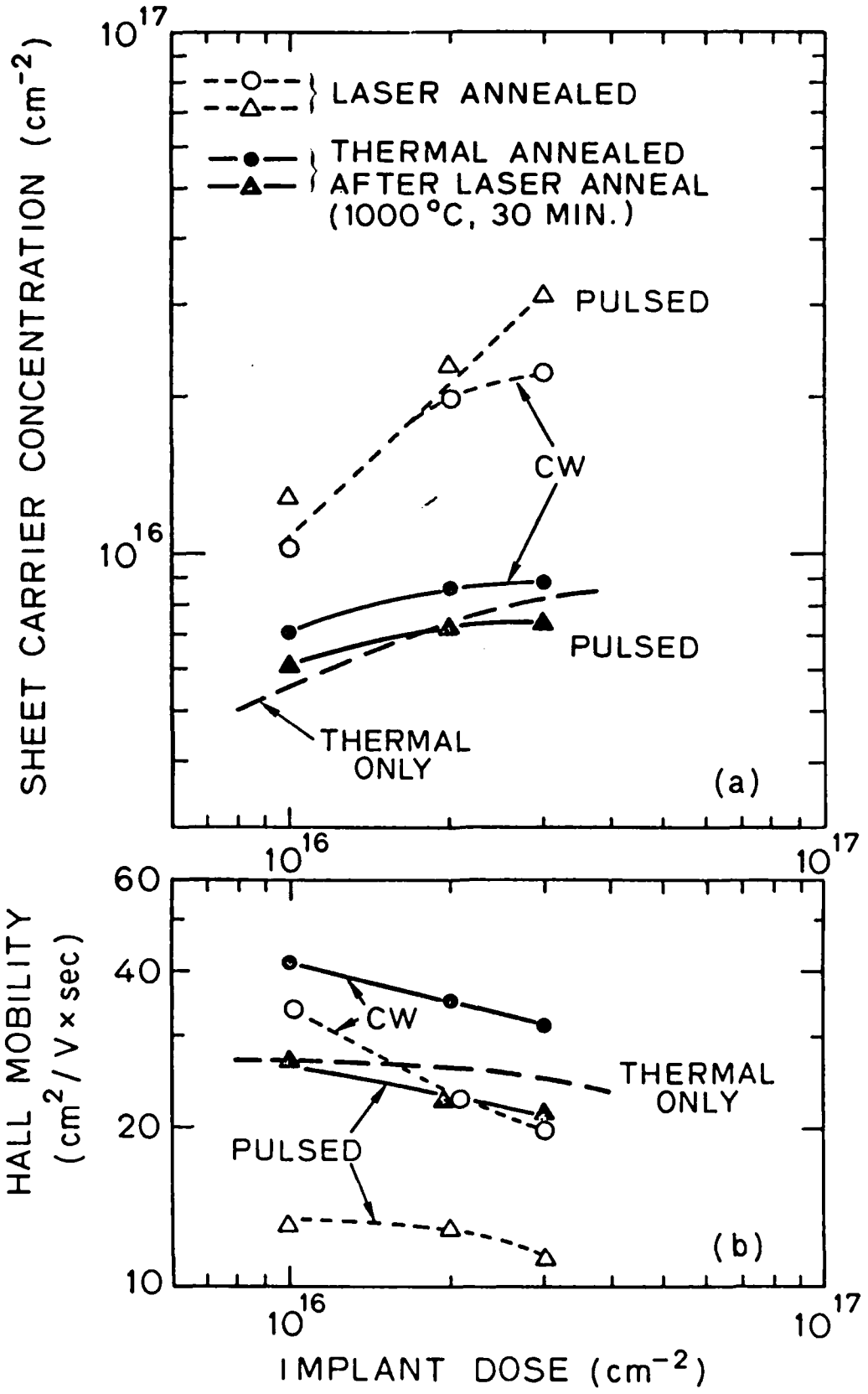
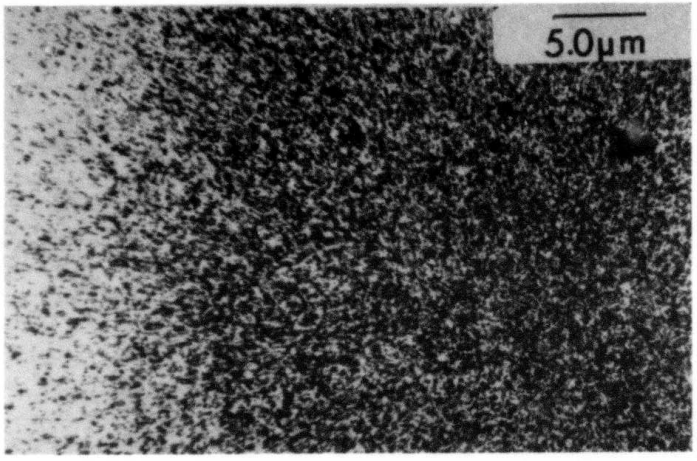
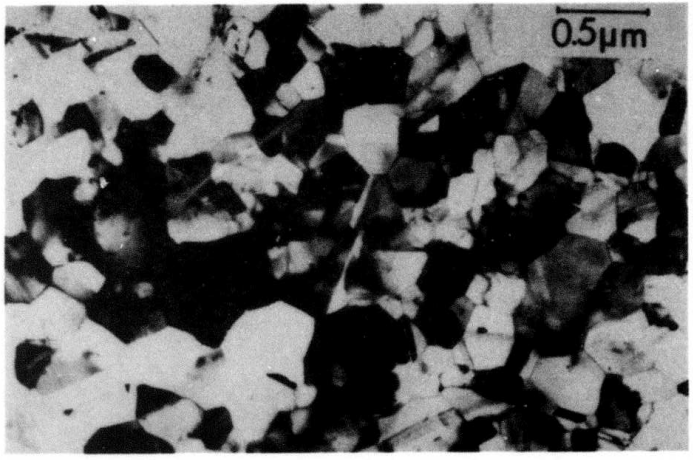

SHEET CARRIER CONCENTRATION (cm^{-2})
10^{17}
10^{16}
LASER ANNEALED
THERMAL ANNEALED
AFTER LASER ANNEAL
(1000°C, 30 MIN.)
PULSED
CW
PULSED
THERMAL
ONLY
(a)
10^{16}
10^{17}
HALL MOBILITY
(cm^2 / V x sec)
60
40
20
10
CW
THERMAL
ONLY
PULSED
(b)
10^{16}
10^{17}
IMPLANT DOSE (cm^{-2})

Fig. 7

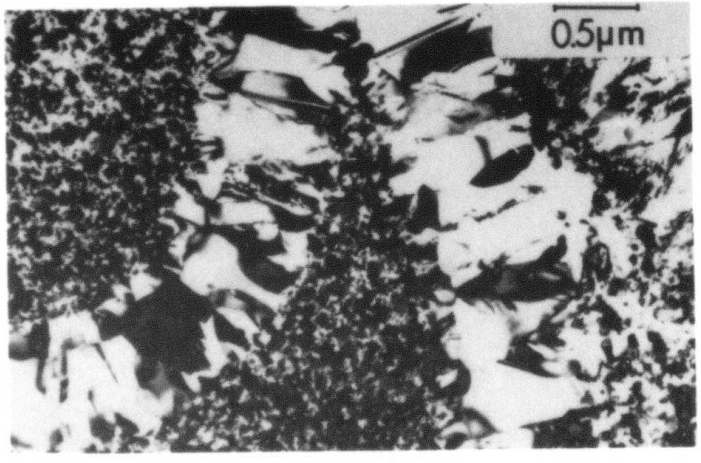


(a)

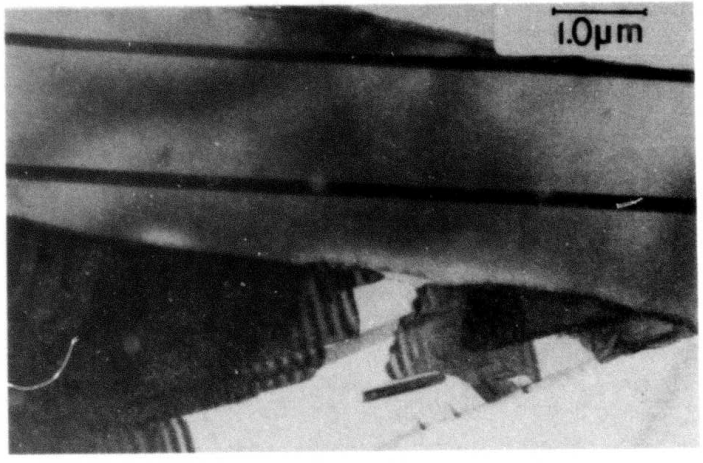


(b)

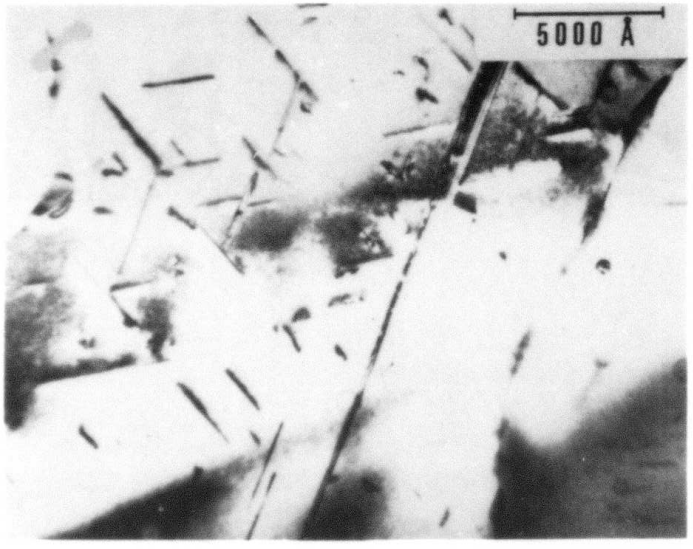
Fig. 8



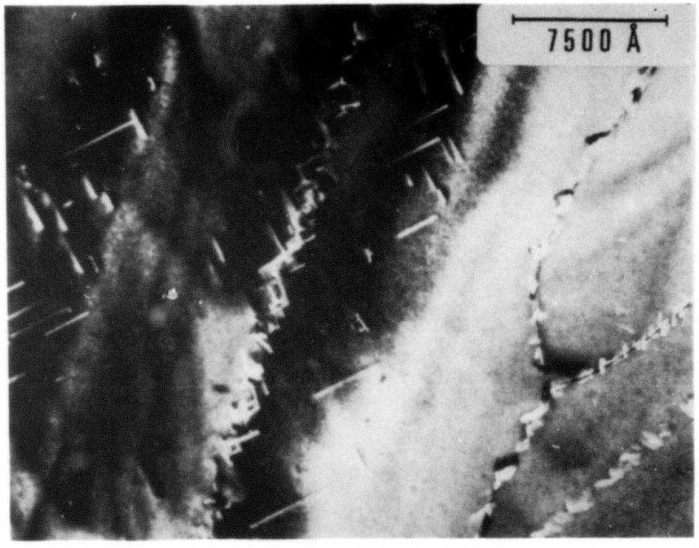
(c)



(d)



(a)



(b)

Fig. 9

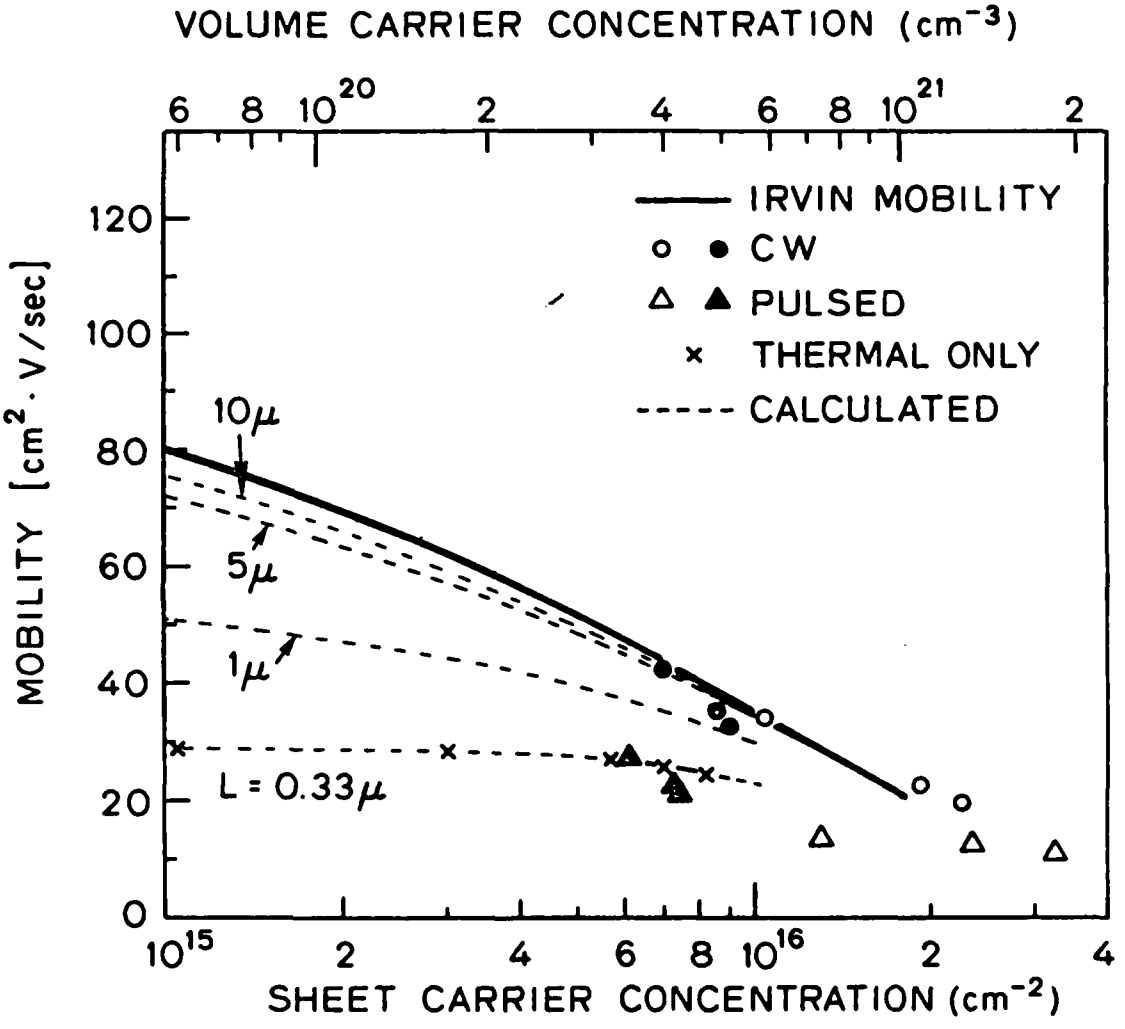

VOLUME CARRIER CONCENTRATION (cm⁻³)
6 8 10²⁰ 2 4 6 8 10²¹ 2
IRVIN MOBILITY
CW
PULSED
THERMAL ONLY
CALCULATED
10μ
5μ
1μ
L = 0.33μ
MOBILITY [cm² · V/sec]
120
100
80
60
40
20
0
10¹⁵ 2 4 6 8 10¹⁶ 2 4
SHEET CARRIER CONCENTRATION (cm⁻²)

Fig. 10

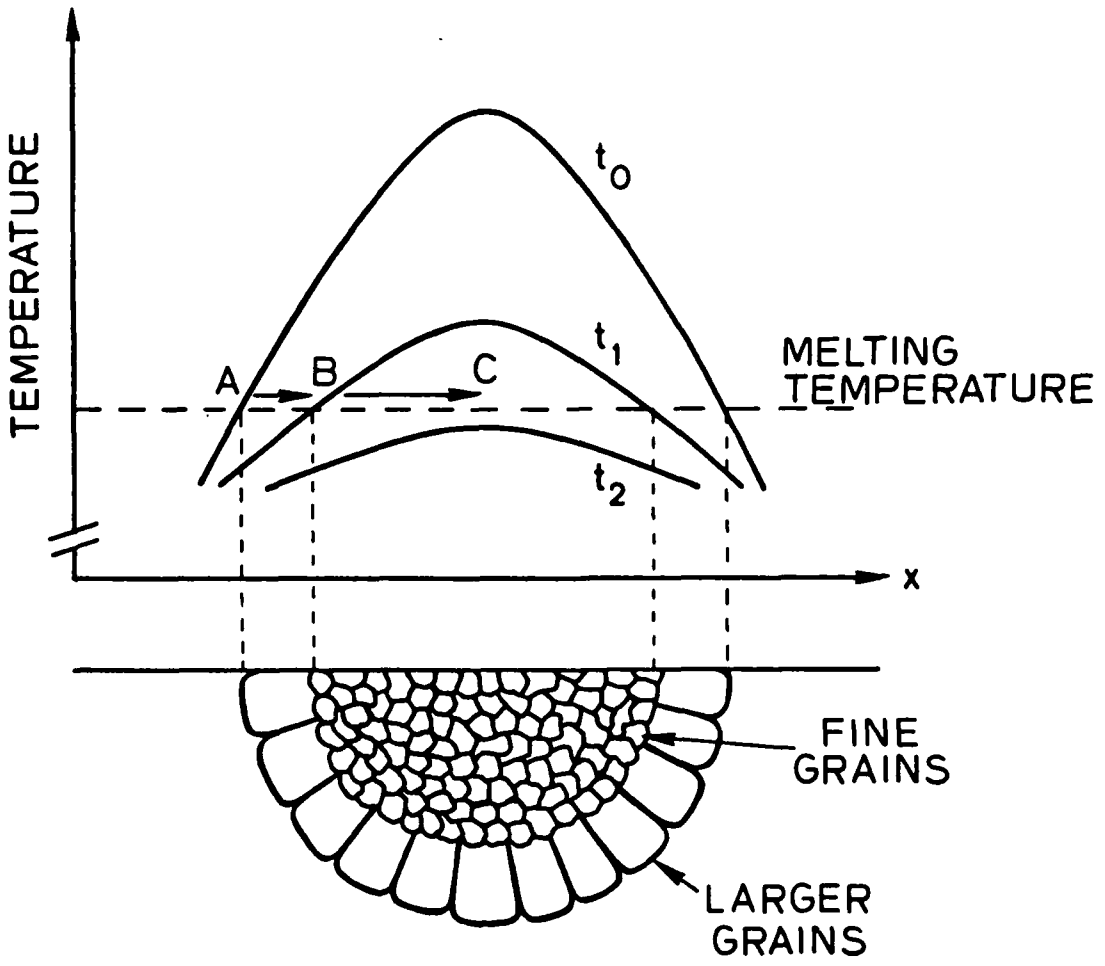

TEMPERATURE
t_0
t_1
t_2
A
B
C
MELTING
TEMPERATURE
x
FINE
GRAINS
LARGER
GRAINS

Fig. 11

Resistivity changes in laser-annealed polycrystalline silicon during thermal annealing

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Polycrystalline silicon layers heavily doped with phosphorus or arsenic were irradiated with a Nd:YAG pulsed laser beam. A 40–50% reduction in sheet resistivity was obtained by laser annealing. However, during subsequent heat treatments the resistivity increased to a value which was higher than the initial value before the laser anneal. The instability of the resistivity is tentatively explained by reprecipitation of dopants both within the grains and at the grain boundaries.

PACS numbers: 72.20.Jv, 81.40.Ef, 79.20.Ds

The deposition of concentrated energy on semiconductor materials using laser or electron beams is of current interest for many semiconductor investigators. Especially the laser annealing of ion-implanted silicon has been very extensively studied.[1-7]

Polycrystalline silicon (poly Si) is a commonly used material for gates and interconnects of MOS integrated circuits, and lowering its resistivity is a basic requirement for high-speed operation of LSI's. Recently, Gat *et al.*[4] reported that cw-Ar laser annealing of poly Si produces a marked increase in grain size, leading to an increase in carrier mobility and a reduciton in sheet resistivity.

We have used a Q-switched Nd-YAG laser to anneal poly Si layers which were heavily doped with phosphorous or arsenic by thermal diffusion. We also obtained reduced resistivity but it was not accompanied by either large grain growth or an increase in carrier mobility, which was reported by previous authors.

In this study, special attention was paid to the resistivity changes in the laser-annealed poly Si during various heat treatments after laser annealing. The changes in surface morphology and grain structure were also investigated by transmission electron microscopy.

A poly Si layer about 3500 Å thick was deposited by thermal decomposition of SiH_4 (silane) at 550 °C onto a 1000-Å thermal oxide which was grown on a p-type (100) silicon wafer. Phosphorus diffusion was performed at 1000 °C from a $POCl_3$ source. Arsenic was diffused in an oxidizing ambient at 1100 °C from a double-layer source (DLS)[9] deposited on top of the poly Si, which consists of a thin (200 Å) As-doped poly Si layer covered with an As-doped silica film 1000 Å thick. Samples which were P or As implanted up to doses of 10^{16} cm^{-2} were also prepared for comparison with the diffused samples.

The laser irradiation was performed with an acoustically Q-switched Nd : YAG laser (1.064 μm). Typical laser parameters were a 10-kHz repetition rate, a 200-nsec pulse length, and an approximately 50-μm optical spot diameter after focusing by a 30-mm lens. The 3-in. wafer was vacuum checked on an x-y stage which was scanned by numerical control. The scan rate was fixed at 80 mm/sec, which resulted in each laser spot being separated by an 8-μm spacing. After each scan, the scanning line was displaced by 10 μm.

The resistivity decreased continuously with increasing laser power, reaching its lowest value at a laser power level between 1.7–2.0 W, which corresponds to a power density of 45–53 MW/cm^2. The laser-annealed area exhibited an easily visible bright region. Careful observations of the region using a Nomarski interference contrast microscope showed miniscus lines formed by successive overlapping laser pulses. At lower laser power, for instance, at 1.0 W, the parallel surface ripples of 1-μm wavelength similar to those reported in Ref. 4 were also observed. These results show that the poly Si actually melts by laser irradiation.

The sheet resistivity of P-diffused poly Si, both before and after laser anneal, is shown in Fig. 1 as a function of diffusion time. Before laser anneal, about 20 min of diffusion at 1000 °C yields the minimum resistivity of 14 Ω/□. Prolonged diffusion does not further lower the value. It is clearly shown that the laser anneal reduces the minimum sheet resistivity by about 40%, namely, to 8 Ω/□. The arsenic-diffused poly Si showed a sheet resistivity of 38–40 Ω/□, nearly independent of the diffusion time, which was varied from

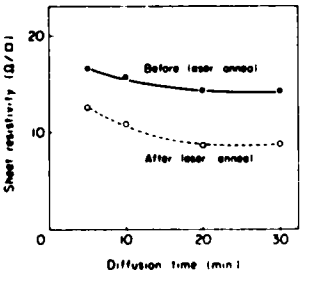

FIG. 1. Sheet resistivity of a 3500-Å-thick poly Si layer, phosphorus diffused at 1000 °C, as a function of diffusion time, before (●) and after (○) laser anneal.

[a]Present address: Stanford Electronics Laboratories, Stanford, Calif. 94305.

 0003-6951/79/010021-03$00.50

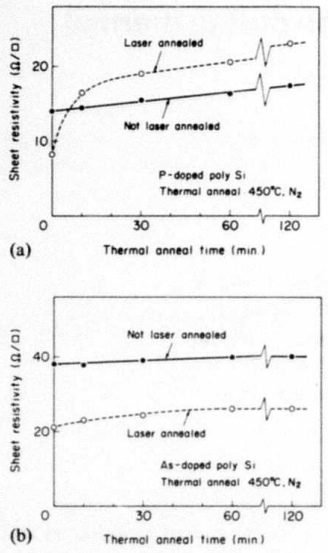

FIG. 2. Sheet resistivity of laser-annealed (○) and unannealed (●) poly Si as a function of subsequent thermal annealing time (450 °C); (a) P-diffused poly Si, (b) As-diffused poly Si. (a) (b)

15–60 min at 1100 °C. The laser anneal also reduced the resistivity to $\approx 20\,\Omega/\square$, or to about 50% of the initial value.

It is of practical importance to study the stability of the resistivity during various heat treatments after laser annealing. Two temperatures, 1000 and 450 °C, were chosen for this study, which are typical temperatures encountered in conventional MOS processing and correspond, for instance, to the phosphorus gettering and postmetallization anneal, respectively. The thermal anneal was performed in N_2 ambient.

The results of a 450 °C thermal anneal are shown in Figs. 2(a) and 2(b). For the P-diffused poly Si [Fig. 2(a)], the resistivity of the laser-annealed sample shows a rapid increase in the first stage of thermal anneal and reaches a value which is *higher* than the initial value before laser anneal. A slight increase in resistivity with increasing thermal annealing time follows, which is also found in the non-laser-annealed sample. The results for the As-diffused poly Si are in marked contrast to those of the P-diffused samples. In this case the resistivity of laser-annealed poly Si does not show the rapid increase at 450 °C that is observed for the P-doped poly Si [Fig. 2(b)]. However, thermal annealing at 1000 °C shows similar instability for both P- and As-diffused samples. At this temperature, the resistivity of the laser-annealed poly Si exceeds the resistivity of unannealed poly Si in the first 10–15 min. No further increase of resistivity with increasing annealing time was found in either laser-annealed or unannealed samples.

Figure 3 shows the changes in surface morphology and grain structure of P-diffused poly Si both before and after laser annealing, and after 1-h thermal anneal at 450 °C following laser anneal. The replica electron micrograph [Figs. 3(a)–3(c)] shows that the mounds which appeared after thermal diffusion disappear as a result of laser anneal, and reappear after thermal annealing. The TEM photographs shown in Figs. 3(d)–3(f) reveal interesting changes in the grain structure. The average grain size of poly Si after P diffusion is about 0.64 μm. The laser irradiation melts the poly Si layer and produces a new structure where the relatively large grains ($\sim$0.7–0.8 μm by $\sim$1.2–1.5 μm) align to form the annular pattern which corresponds to the miniscus lines discussed previously. The regions both inside and outside of the annular pattern consist of a matrix of small grains of average size 1200 Å. The thermal annealing after laser anneal does not change the structure essentially, and only the small grains show a slight increase in grain size to about 2000 Å. The results for the As-diffused poly Si were almost the same except for the fact that the mounds did not reappear after a 1-h thermal anneal at 1000 °C.

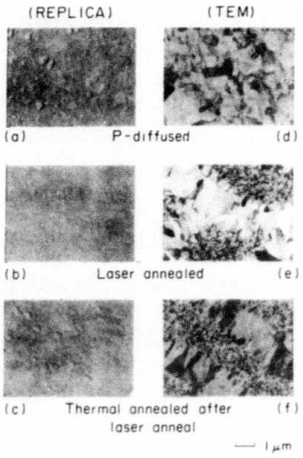

FIG. 3. Replica electron micrographs [(a)–(c)] and transmission electron micrographs [(d)–(f)] of P-diffused poly Si, both before and after laser anneal, and after a 1-h subsequent thermal anneal at 450 °C.

The changes in the carrier mobility and the carrier concentration of the P-doped poly Si are shown in Fig. 4. The mobility does not essentially change, and only the carrier concentration changes drastically by laser annealing and by thermal annealing after laser anneal. These results are quite different from those obtained by Gat *et al.*, where the mobility is increased by laser annealing.

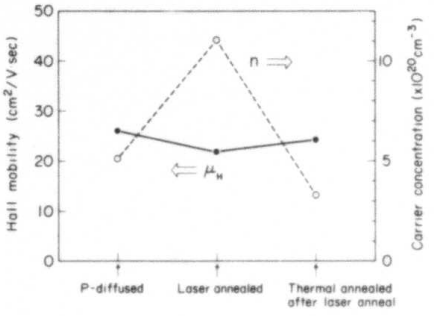

FIG. 4. Hall mobility and carrier concentration changes in P-diffused poly Si caused by laser annealing and by thermal annealing after laser anneal.

The carrier concentration after P diffusion is about one-half order smaller than the phosphorus concentration in poly Si ($\approx 1.6\times 10^{21}$) measured by Auger electron spectroscopy, which suggests that a considerable amount of phosphorus is probably precipitated at grain boundaries. The laser irradiation causes melting of the poly Si after which phosphorus atoms are incorporated in substitutional sites during recrystallization. This process appears to cause phosphorus atoms near the grain boundaries to become electrically active, thus reducing the sheet resistivity. The activated impurities may, however, be thermodynamically unstable if their concentration is sufficiently high. In this case they tend to form electrically inactive precipitates during subsequent thermal annealing, which accounts for the rapid increase in sheet resistivity during thermal annealing.

Recently, Lietoila *et al.*[10] observed a similar thermal instability in high-dose (7×10^{15} cm^{-2}) As-implanted cw laser-annealed single-crystal silicon. They pointed out that the maximum active arsenic concentration relaxes to 3×10^{20} cm^{-3} during thermal annealing, and excess arsenic atoms form small rod-shaped precipitates aligned along $\langle 001\rangle$, $\langle 010\rangle$, $\langle 01\bar{1}\rangle$, and $\langle 011\rangle$ directions.

The same precipitation process can be expected to occur in the grains of poly Si film where excess phosphorus atoms were activated by pulsed-laser irradition. The driving force for the rod-shaped precipitate formation may be the strain in the crystal induced by excess impurity activation and thus would be impurity-concentration dependent. Our failure to observe thermal instability at 450 °C in As-doped poly Si might be explained by the smaller strain due to the arsenic concentration [$(3.5\text{–}4)\times 10^{20}$ cm^{-3}] compared to the P-doped poly Si where more than 10^{21} cm^{-3} phosphorus atoms were activated by laser anneal. In addition to the precipitation process within the grains, the precipitation might occur also at grain boundaries. The large number of small grains shown in Fig. 3(e), which were produced by laser annealing, provide a large number of sinks for impurity atoms. Precipitation on grain boundaries can explain the increase in resistivity in excess of the pre-laser-anneal value.

It should be noted that the results are not the characteristics of the thermally diffused sample because the similar instability is also observed in the P- or As-implanted and laser-annealed poly Si.

The authors are pleased to acknowledge their indebtedness to Professor W. Tiller, A. Lietoila, and K.F. Lee of Stanford University for valuable discussions, to T. Yoshii and H. Yako (Toshiba Corp.) for the electron microscope observations, and to T. Inoue (Toshiba Corp.) for Auger measurements. One of us (J.F. Gibbons) wishes to acknowledge ARPA (Contract MDA903-78-C-0128) for supporting this work.

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Crystal structure and thermal oxidation of laser-recrystallized polycrystalline silicon

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Laser-recrystallized polycrystalline silicon exhibits a weak ⟨111⟩ preferred orientation, in contrast to the strong ⟨110⟩ texture seen in fine-grain poly-silicon. The oxide thickness thermally grown on laser-recrystallized poly-silicon is much greater than that on fine-grain poly-silicon when both are heavily phosphorus doped but is approximately the same when both films are lightly doped.

PACS numbers: 81.40.Ef, 61.50.Jr, 81.60. – j, 79.20.Ds

Although the fabrication of metal-oxide-semiconductor field-effect transistors (MOSFET's) with their active channels in a layer of polycrystalline silicon was investigated some time ago,[1] the device properties were greatly inferior to those of transistors fabricated in single-crystal silicon because of the small grain size and high trap density. Recently, the technique of laser melting and recrystallization of poly-silicon[2] has allowed the fabrication of MOSFET's with their active channels in the large grains formed by laser recrystallization.[3,4] The transistor properties of these devices have been found to approach those of devices fabricated in single-crystal silicon.

Transmission electron microscopy has shown that long grains of dimensions approximately $2 \times 20\,\mu$m are formed under optimum conditions.[2] The early study suggested that the grains had a mixture of crystal orientations. In this letter the structural changes caused by laser recrystallization will be examined more quantitatively by x-ray diffraction, and the effect of the heat treatment often used before laser recrystallization will also be investigated. Poly-silicon films deposited both on silicon dioxide and on silicon nitride will be considered. Since the thickness of the oxide subsequently formed during device fabrication may depend on the structure of the poly-silicon, the thermal oxidation of laser-recrystallized poly-silicon will also be briefly examined.

Lightly doped, p-type, ⟨111⟩ oriented silicon wafers were used as substrates in this experiment. Some were thermally oxidized at 1000 °C in a TCE/O_2 ambient to obtain an oxide thickness of 1000 Å, while others were coated with 1000 Å of low-pressure CVD silicon nitride. Films of low-pressure CVD poly-silicon about 5500 Å thick were then deposited at 625 °C on both types of substrate. Some samples

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of each type were thermally annealed at 1100 °C in a nitrogen ambient since this heat treatment has been found to ease control of the laser recrystallization process. The samples were then laser processed at Stanford University with a cw scanning argon laser to melt and recrystallize the poly-silicon films as described previously,[2] forming a large-grain structure in most cases. A focusing lens of 135-mm focal length was used, resulting in a beam diameter of about 40 μm. Each scanned line was stepped 18 μm from the previous line. A sample-holder temperature of 350 °C was used. The samples were then returned to Hewlett-Packard for further processing and evaluation.

A conventional x-ray diffractometer was used. Measurements were taken with the samples mounted both parallel and perpendicular to the laser scan direction, but no anisotropy was seen. The results reported are the average of the two measurements. The intensities of the signals from the {111}, {220}, {311}, {400}, and {331} peaks were measured and normalized to indicate the relative amount of crystallites with ⟨111⟩, ⟨110⟩, ⟨311⟩, ⟨100⟩, and ⟨331⟩ orientation in each film. The measured signals were normalized to account for the signal strengths expected in a thick, randomly oriented sample, and also for the finite film thickness.[5]

While the surface structure observed in poly-silicon by optical microscopy does not always correlate with the grain structure, some general observations can be made from Table I and Fig. 1. The films which were not laser processed had a fine-grain appearance. Those laser processed, but not thermally annealed (14-1, 16-1, 16-3) appeared to have a featherlike, long-grain structure, while those which were also thermally annealed (13-3, 15-1) indicated a large-grained appearance on the surface. One sample (13-1) indicated a less regular appearance, probably related to a mixed structure obtained because of less complete recrystallization.

The normalized x-ray results are also shown in Table I. As expected,[5] the ⟨110⟩ orientation is dominant in all the films immediately after deposition, with the normalized intensity being about ten times larger than that from any other orientation. Thermally annealing the samples at 1100 °C decreases the preference for ⟨110⟩ texture, although this orientation is still dominant. The ⟨111⟩, ⟨311⟩, and ⟨311⟩ orientations all increase significantly, with little difference seen between the films deposited on silicon nitride and those deposited on silicon dioxide.

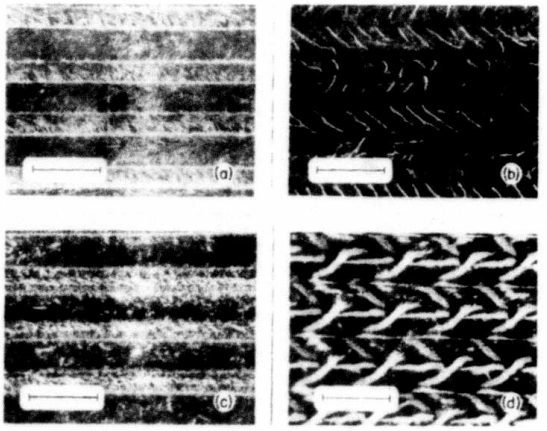

FIG. 1. Dark-field photomicrographs of laser-recrystallized poly-silicon on Si_3N_4 [(a) and (b)] and on SiO_2 [(c) and (d)]; (b) and (d) show samples thermally annealed before laser recrystallization. Markers are 50 μm long.

Laser recrystallization of the poly-silicon films deposited on silicon nitride decreases the amount of ⟨110⟩ texture significantly; the crystallites with ⟨111⟩ and ⟨311⟩ orientation increase especially, with the ⟨111⟩ being generally dominant. Similar trends are seen on both samples which were thermally annealed and those which were not, with the thermally annealed samples showing an especially marked decrease in the ⟨110⟩ texture but little further increase in the ⟨331⟩ texture.

The poly-silicon films deposited on silicon dioxide and not thermally annealed showed the same trends as those deposited on silicon nitride, with, perhaps, somewhat less pronounced changes; there was less decrease in the ⟨110⟩ texture and less increase in the ⟨311⟩ texture. This difference may be partially related to the different laser recrystallization conditions, which were optimized for each type of insulator. The thermally annealed sample which was laser recrystallized to produce a large-grain structure (13-3) also

TABLE I. Preferred orientation in laser-recrystallized poly-silicon.

Sample	Insulating film	Thermal anneal	Laser processing	Laser power (W)	Grains	Normalized x-ray texture ⟨111⟩	⟨110⟩	⟨311⟩	⟨100⟩	⟨331⟩
16-U	Si_3N_4	no	no	...	fine	25	720	78	0	~58
16-1	Si_3N_4	no	yes	8	long	335	133	363	~156	168
16-3	Si_3N_4	no	yes	10	long	445	183	342	~135	174
15-U	Si_3N_4	yes	no	...	fine	250	478	200	0	194
15-1	Si_3N_4	yes	yes	8	large	395	68	308	208	219
14-U	SiO_2	no	no	...	fine	50	615	62	0	~65
14-1	SiO_2	no	yes	8	long	365	379	262	198	245
13-U	SiO_2	yes	no	...	fine	258	491	150	~83	226
13-1	SiO_2	yes	yes	8	mixed	193	595	249	167	168
13-3	SiO_2	yes	yes	11	large	485	234	275	260	194

showed similar trends to those found on the silicon-nitride-containing sample. The other sample (13-1) was treated at a lower laser power so that the large-grain structure was not obtained, and the film probably contained a mixture of large and small grains. The increase in the amount of ⟨110⟩ texture is probably related to some growth of the structure initially found in the as-deposited films. This mixed case is, of course, of less interest than the fully recrystallized films.

A significant increase in ⟨100⟩ texture is seen in many cases, but in no case does ⟨100⟩ become the dominant orientation. In general, the laser-recrystallized samples exhibit less-strong preferred orientation than do the as-deposited films. The presence of this mixed orientation may significantly influence the oxidation rate and interface charges of structures containing laser-recrystallized poly-silicon.

To complement the structural investigation, a brief experiment was conducted to determine the oxide thickness grown on laser-recrystallized poly-silicon under conditions which might be used in an integrated-circuit process. During this portion of the investigation, only poly-silicon films deposited onto silicon nitride with no subsequent nitrogen anneal were studied. After laser recrystallization, some of the wafers were doped by a 950 °C, $POCl_3$ predeposition which produced a sheet resistance of 10 $\Omega/\square$ in single-crystal silicon. Both undoped and doped films were then oxidized.

Two different oxidation cycles were used. A 125-min, 1000 °C TCE/O_2 oxidation, which forms 1000 Å of oxide on ⟨100⟩ oriented, single-crystal silicon, was used in some cases. A 210-min, 800 °C steam oxidation was also investigated in order to emphasize the effects of the silicon orientation and structure. The oxide thicknesses were measured on the poly-silicon and single-crystal control wafers with a uv spectrophotometer.[6] After the oxide thicknesses were measured, the oxidation cycles were repeated without stripping the oxide so that thicker oxides, which could be measured more easily, were grown.

The oxide thicknesses after the first oxidation cycle are shown in Table II. The oxide thicknesses grown on the undoped poly-silicon with the 1000 °C TCE/O_2 oxidation fall between those on the ⟨100⟩ and ⟨111⟩ oriented, single-crystal silicon oxidized simultaneously, being about 6% greater than that on ⟨100⟩ oriented silicon after the first oxidation. After the second oxidation the oxide thicknesses continued to fall between those of the two orientations of single-crystal silicon. Oxidation under these conditions is influenced by diffusion of oxygen through the already formed oxide, as well as by surface reaction, so the effect of the silicon structure and orientation is small.

The 800 °C steam oxidation is controlled primarily by the surface reaction so the effects of orientation and structure should be more significant, as observed, with the oxide thickness on ⟨111⟩ oriented, single-crystal silicon 46% greater than that on ⟨100⟩ silicon. The oxide thickness on the fine-grain poly-silicon appears to be slightly greater than that on ⟨110⟩ silicon, with the oxide on the laser-annealed regions probably even slightly thicker. Thus the oxide thickness grown on undoped, laser-recrystallized poly-silicon under surface-reaction-controlled conditions differs only slightly from that on fine-grain poly-silicon and is similar to that on the fast-oxidizing orientations of single-crystal silicon.

The influence of the laser recrystallization on heavily phosphorus doped poly-silicon is more dramatic. Under these conditions, the oxidation rate is controlled by the dopant concentration at the surface, and the effect of crystal orientation is less significant, as can be seen by comparing the oxide thicknesses on the two orientations of doped, single-crystal silicon in Table I. The oxide thickness on the doped, fine-grain poly-silicon is markedly less than that on the single-crystal silicon or on the laser-recrystallized poly-silicon, while that on the laser-recrystallized poly-silicon is close to that on the single-crystal silicon.

Thinner oxides on heavily doped, fine-grain poly-silicon than on simultaneously doped single-crystal silicon have been observed before and have been related to the lower active dopant concentration near the surface of the poly-silicon.[6] During the doping cycle, the dopant can diffuse farther into the poly-silicon than into the single-crystal silicon so that the average surface concentration is lower, and the oxide subsequently grown is thinner. In addition, even if the dopant-atom concentration were the same, the lower electrical activity in the poly-silicon would keep the Fermi level closer to midgap so that the dopant-enhanced oxidation would not be as significant.

Similar reasoning can account for the thicker oxide grown on the laser-recrystallized poly-silicon than on fine-grain poly-silicon. The dopant appears to diffuse away from the surface of the laser-recrystallized poly-silicon at about the same rate as in single-crystal silicon and less rapidly than in fine-grain poly-silicon since grain-boundary diffusion is less important; consequently, the oxide grown is thicker than on fine-grain poly-silicon.

While fine-grain poly-silicon films exhibit a strong ⟨110⟩ preferred orientation, the preference for a particular orientation is less pronounced in laser-recrystallized poly-silicon, although there is some preference for ⟨111⟩ orienta-

TABLE II. Oxide thickness on laser-recrystallized poly-silicon

Doping	Oxidation temperature (°C)	Oxidizing ambient	Oxide thickness (Å)				
			Poly-silicon		Single-crystal silicon		
			Recrystallized	Fine-grain	⟨100⟩	⟨111⟩	⟨110⟩
undoped	1000	TCE/O	1050	1060	980	1100	~1120
undoped	800	steam	1930	1830	1140	1670	1770
phosphorus doped	800	steam	6190	4830	6030	6800	

tion. The oxide thickness grown on lightly doped, laser-recrystallized poly-silicon is not greatly different from that on fine-grain poly-silicon and is probably dominated by the fast-oxidizing orientations under surface-reaction-controlled conditions. The oxide thickness on heavily doped, laser-recrystallized poly-silicon is similar to that on single-crystal silicon and is much greater than that on fine-grain poly-silicon.

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Charges at a Laser-Recrystallized-Polycrystalline-Silicon/Insulator Interface

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Abstract—**Capacitance-voltage characteristics have been measured to determine the interface properties at the back surface of a layer of laser-recrystallized polycrystalline silicon. The interface between the recrystallized poly-silicon and an underlying oxide layer can be characterized by an effective fixed-charge density and a fast-state density, both in the low-to-middle-10^{11} cm^{-2} range. Charge trapping at a poly-silicon/silicon-nitride interface precludes the determination of a meaningful value of interface charge.**

Introduction

A recent report [1] has described the fabrication of MOS transistors with their active channels within a layer of laser-recrystallized polycrystalline silicon. The possibility of obtaining useful semiconductor devices in poly-silicon offers the opportunity for constructing new device structures, as well as removing some of the limitations encountered with conventional devices in single-crystal silicon. The characteristics of devices fabricated in laser-recrystallized poly-silicon films will be strongly dependent on the properties of the interface between the poly-silicon film and the underlying insulator. In conventional silicon-gate MOS applications, the polysilicon is very heavily doped, and the poly-silicon near the insulator is never depleted. When the active element of a device is placed in the laser-recrystallized poly-silicon film itself, the film is only moderately doped, so that depletion and inversion layers can easily be formed by charges in the insulator or at the poly-silicon/insulator interface. In order to investigate the behavior of this interface, capacitor structures were fabricated, and capacitance-voltage measurements were made with the depletion regions extending into films of moderately doped, laser-recrystallized poly-silicon. Both thermally grown silicon dioxide and low-pressure CVD silicon nitride were investigated as the insulating layer.

Experimental Structures

All of the structures to be studied (Fig 1) were fabricated on 0.01 Ω−cm, n-type silicon wafers, which subsequently served as the gate electrode. A 1000 Å-thick, TCE/O_2 gate oxide was grown on some wafers at 1000°C, while others were covered with 1000 Å of low-pressure CVD silicon nitride. A 5500 Å-thick film of LPCVD poly-silicon was then deposited at 625°C on all wafers. The wafers which contained an oxide layer were next annealed at 1100°C in N_2 for one hour to ease control of the subsequent laser recrystallization process, while the wafers which contained a nitride layer did not require this thermal anneal. All poly-silicon films were implanted with $1x10^{12}$ boron ions cm^{-2} at 100 keV. Portions of each wafer were then recrystallized with a scanning cw argon laser, as described previously [2]. The substrate temperature was held at 350°C, and the power of the approximately 70 μm-diameter laser beam was varied, with different laser powers being used on different regions of each wafer. At the higher laser powers the poly-silicon was melted, both activating and redistributing the dopant and forming a large-grained structure in the poly-silicon. Aluminum was then deposited and defined into squares 300 or 900 μm on a side; the aluminum served as a contact to the poly-silicon "substrate". The poly-silicon was plasma etched using the metal as a mask. After a final 450°C H_2 anneal, the high-frequency (1 MHz), capacitance-voltage characteristics were measured, with the depletion regions extending into the poly-silicon. To facilitate discussion, all "gate" voltages mentioned in the discussion below are those applied to the n^+ single-crystal wafer which served as the gate electrode.

Results and Discussion

The structures with silicon dioxide beneath the poly-silicon will be considered first. Laser powers of 14-16 W produced overlapping scans and the desired large-grain structure in the poly-silicon. In the laser-recrystallized areas well-defined accumulation and inversion regions are observed in the capacitance-voltage characteristics. The capacitance with the poly-silicon surface accumulated corresponds to an oxide thickness very close to the 1000 Å target thickness. When the opposite polarity voltage is applied, the capacitance decreases to a value indicating a depletion region approximately 2000 Å wide in the poly-silicon. This polarity voltage also tends to deplete the n^+ gate wafer, but the heavy doping in this wafer increases the voltage necessary for significant depletion and also limits the width of the depletion region so that the effect of depletion into the n^+ wafer can be neglected in the following discussion.

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The depletion-region width in the poly-silicon corresponds to a dopant concentration of approximately (2.2 -2.6)x10^{16} cm^{-3}, confirming that virtually all the dopant is activated by the laser recrystallization. The dopant concentration is somewhat higher than the average dopant concentration of 1.8 x 10^{16} cm^{-3} expected if all the 1 x 10^{12} cm^{-2} boron atoms implanted were active and were uniformly distributed through the 5500 Å-thick poly-silicon film. (Laser recrystallization does not appear to change the average film thickness.) This anomalously high apparent concentration may possibly be related to dopant segregation near the bottom of the poly-silicon film as it recrystallizes or to residual defect stages which limit the depletion-region width.

In the regions of the same wafer not affected by the laser, the minimum capacitance is considerably less than in the recrystallized regions, corresponding to a maximum depletion-region width of about 4500 Å, close to the thickness of the poly-silicon film, suggesting that the high resistance of the unaffected poly-silicon may cause the entire thickness of the film to act as a dielectric when attempts are made to deplete the surface. (Aluminum from the deposited electrode may have penetrated into the poly-silicon slightly, causing the apparent maximum depletion-region width to be slightly smaller than the poly-silicon film thickness.) Samples which received neither the 1100°C thermal anneal nor the laser processing showed very little dependence of the capacitance on the gate voltage.

After a negative bias-temperature stress to insure that any positive mobile ions present did not influence the results, the flatband voltage in the laser-recrystallized regions was found to be in the range -2.9 to -3.4 V. If ϕ_{MS} is taken to be -0.90V, the fixed-charge density is calculated to be about 4 x 10^{11} cm^{-2}, which is somewhat higher than that expected in single-crystal silicon but not unreasonable since the processing was not optimized for this unconventional structure. (X-ray measurements indicate a crystal structure containing grains of various orientations, with a weak preference for (111) orientation under the conditions employed here [3], so that the minimum fixed-charge density would be higher than that expected for (100) silicon,)

The voltage between the measured flatband and inversion points of the C-V characteristic was greater than calculated, however, suggesting the presence of some fast states or lateral nonuniformities. If this distortion in the curve were entirely related to fast states, their density between flatband and inversion would be about 2 x 10^{11} cm^{-2}. A portion of the distortion in the C-V characteristic may be related to nonuniformities since a region treated under conditions which produced incompletely overlapped recrystallized regions, showed distorted C-V characteristics corresponding to a parallel combination of the recrystallized and unaffected curves.

In the regions which were not affected by the laser, the magnitude of the flatband voltage varied significantly and was generally greater than 10V, suggesting an effective charge density greater than 10^{12} cm^{-2}.

Thus, the properties of the silicon-dioxide/poly-silicon interface under a layer of laser-recrystallized poly-silicon resemble, but are inferior to, those at the interface between a thermally grown oxide and single-crystal silicon. This interface is, however, of much higher quality than most semiconductor-insulator interfaces not formed by thermal oxidation. For example, the interface between single-crystal silicon and a deposited oxide layer is generally unstable and can, at best, be characterized by very high fixed-charge and interface-state densities.

Capacitors containing an insulating layer of silicon nitrite were also tested. The poly-silicon deposited on the silicon nitride contained a wide range of crystal structure after laser recrystallization depending on the laser power used, which varied from 14 to 17 W. No long grains were seen at the lowest power, while the highest power produced totally overlapped recrystallized regions containing long grains. The capacitance-voltage characteristics were also quite different in regions annealed at different powers.

In all cases, the maximum capacitance corresponded to a silicon-nitride layer with a relative permittivity of 7.0 for the 1000 Å thickness deposited. The behavior of the capacitance-voltage characteristics in depletion was markedly different in the differently processed regions (Fig. 2). The minimum value of capacitance was lowest in the region recrystallized at the lowest power (approximately 44% of the nitride capacitance); the minimum capacitance increased with increasing laser power to about 60% of the nitride capacitance for the highest laser power. In addition, at large positive gate voltages (> 30 V) (in the direction tending to invert the poly-silicon), the capacitance again increased toward its maximum value, suggesting the presence of a source of minority carriers to charge the inversion layer rapidly. In the region processed at the lowest laser power, there was no flat portion of the C-V curve at the minimum capacitance. As the laser power and the minimum capacitance increased, a flat region developed in the C-V characteristic. (Rapid minority-carrier generation was also seen in samples with a silicon-dioxide insulator at high positive gate voltages.)

This behavior of the minimum capacitance would not be consistent with defects within the poly-silicon film, since a higher defect concentration at higher laser powers would have to be postulated, in contrast to the reduced defect density expected as the long-grain structure becomes more fully developed.

No meaningful value of the fixed-charge or fast-state density can be extracted from the capacitance-voltage measurements because of electron trapping in the insulator. Even before a bias-temperature stress, the flatband voltage changes significantly when large voltage ramps are applied. (In contrast, no change was seen in samples containing a silicon-dioxide insulator when tested with similar, high-magnitude voltages.)

Limited tests indicated no significant improvement by laser annealing the nitride before the poly-silicon was deposited, in addition to recrystallizing the poly-silicon with the laser after the poly-silicon deposition. The results obtained from the structures containing silicon nitride show that the poly-silicon/silicon-nitride interface is not well behaved, a situation similar to that of a silicon-nitride/single-crystal-silicon interface.

Summary

Capacitance-voltage characteristics have been measured to determine the interface properties at the back surface of a layer of laser-recrystallized poly-silicon. The interface between the recrystallized poly-silicon and an underlying oxide layer can be characterized by an effective fixed-charge density and a fast-state density, both in the low-to-middle-10^{11} cm^{-2} range. The poly-silicon/silicon nitride interface is not as well behaved. The minimum capacitance depends on the laser power used to recrystallize the poly-silicon, and charge trapping at the interface precludes the determination of a meaningful value of interface charge.

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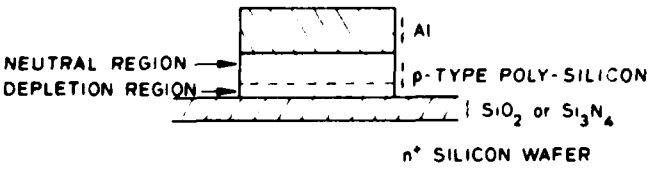

Fig. 1. Cross section of experimental capacitor structure, showing depletion region extending into the poly-silicon when a "gate" voltage is applied to the n+ wafer.

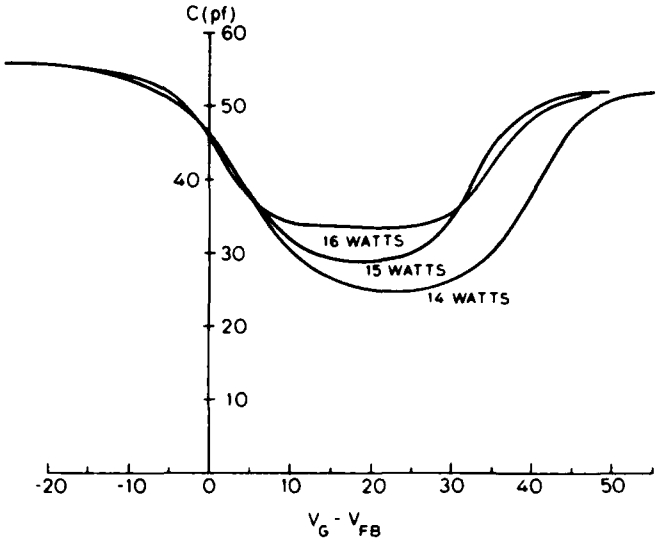

Fig. 2. Experimental capacitance-voltage characteristics of structures containing a silicon-nitride insulator under poly-silicon films recrystallized at three different laser powers.

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INTERFACE CHARGES BENEATH LASER-ANNEALED INSULATORS ON SILICON

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Abstract—Laser annealing of a thermally grown, silicon-dioxide layer reduces an initially high fixed-charge density. Similar annealing of a silicon-nitride-covered silicon wafer does not markedly improve the interface characteristics. Laser melting and recrystallization of polycrystalline silicon above a thermally grown oxide does not appreciably increase the interface charges at the underlying silicon-dioxide/single-crystal-silicon interface.

INTRODUCTION

The characteristics of MOS transistors are strongly dependent on the properties of the silicon-insulator interface. Fixed charge changes the threshold voltage of the transistor while fast states degrade its transconductance and subthreshold behavior. When unconventional processing is employed, the effect of the process on these charges must be determined. Since laser annealing of MOS structures and laser recrystallization of polycrystalline-silicon gate electrodes are being contemplated, the effect of laser processing on MOS device behavior must be assessed. High interface-charge densities may be reduced by energy from the laser beam allowing the relaxation of strained bonds by either thermal processes or, more directly, by photon-defect interactions. On the other hand, low interface-charge densities may possibly increase if the laser energy breaks bonds at the interface rather than allowing them to relax further.

In an attempt to determine the effect on MOS characteristics of processing with a *cw* scanning argon laser, several different types of MOS capacitors were fabricated, and the capacitance–voltage characteristics were measured. The effect of laser annealing on the charges at an insulator/single-crystal interface are reported here. All three different structures examined in this experiment (Fig. 1) were fabricated on 1–3 Ωcm, (100)-oriented, *n*-type silicon wafers so that the depletion regions extended into the silicon substrate.

The first experiment was designed to determine if laser melting and recrystallization of a poly-silicon gate electrode would degrade the interface characteristics at an underlying silicon-dioxide/single-crystal-silicon interface. To fabricate this structure (Fig. 1a), a 5500 Å-thick layer of low-pressure CVD polysilicon was deposited at 625°C onto a 1000 Å-thick, TCE/O_2 gate oxide; the polysilicon was next annealed at 1100°C in N_2 and then phosphorus doped at 950°C from a $POCl_3$ source. (The high-temperature nitrogen anneal makes control of the laser parameters less critical[1], probably by affecting the top surface of the polysilicon. A wider range of laser power can be used to recrystallize the polysilicon after the thermal anneal without agglomeration of the molten silicon). Portions of each wafer were then laser processed to melt and recrystallize the polysilicon, forming a large-grain structure as described previously[2]. A laser power of 8 W was used with a focusing lens of 135 mm focal length, resulting in a beam diameter of ~40 μm on the sample. A sample-holder temperature of 350°C was used. The sheet resistance of the recrystallized polysilicon was 7–9 Ω/□, compared to 12 Ω/□ for the original, fine-grain polysilicon. Aluminum was then deposited and defined to form squares 300 and 900 μm on each side. The polysilicon was plasma etched, and the structure was annealed at 450°C in a hydrogen ambient before the high-frequency (1 MHz), capacitance-voltage characteristics were measured. All measurements quoted were taken after a negative bias-temperature stress to ensure that any mobile ions which may have been present would not affect the magnitude of the charges measured.

The processing employed assured low interface-charge densities, as found in high-quality MOS transistors, and the experiment was undertaken to see if laser melting of

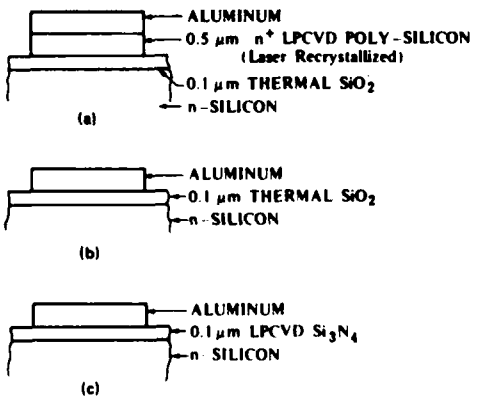

Fig. 1. Cross sections of the three experimental structures used in this investigation.

the polysilicon would degrade the devices by disrupting bonds at the $Si-SiO_2$ interface, with a consequent increase in the interface charges. The fixed-charge density was found to be in the mid-$10^9\,cm^{-2}$ range on devices located outside of the laser-recrystallized regions of the polysilicon and also on control wafers which were not exposed to the laser, with an average value of $(6.2 \pm 3.1) \times 10^9\,cm^{-2}$. The fixed-charge density was consistently increased to the mid-$10^{10}\,cm^{-2}$ range by laser melting of the polysilicon, with an average value of $(3.4 \pm 1.0) \times 10^{10}\,cm^{-2}$. These values correspond to voltages of 0.03 and 0.17 V, respectively, for the present 1000 Å-thick oxide, and the former is probably within the uncertainty of the data reduction. No distortion was seen in the shape of the $C-V$ curve after laser processing, with both the recrystallized and unexposed regions showing the characteristic expected when no appreciable fast-state density is present. (The 0.1 V resolution of the measurement technique indicates that the fast-state density between flatband and inversion was less than about $2 \times 10^{10}\,cm^{-2}$). From these results, we may, therefore, conclude that laser recrystallization of a polysilicon gate does not appreciably increase the interface-charge densities at the underlying silicon-dioxide/single-crystal-silicon interface, although a slight increase in the fixed-charge density is seen.

The other structures considered in this investigation did not involve polysilicon. The second experiment was designed to determine if laser annealing would reduce a moderately high fixed-charge density at a silicon-dioxide/single-crystal-silicon *interface*. In this experiment (Fig. 1b), a 1000 Å-thick, TCE/O_2 gate oxide was grown at 1000°C and thermally annealed at 1100°C in N_2 before laser annealing. The processing employed assured a moderately high fixed-charge density. The wafers were then laser annealed with laser powers varying from 7 to 12 W with a focusing lens of 250 mm focal length, resulting in a beam diameter of approximately 70 μm on the sample. Aluminum was next deposited and defined to form aluminum-gate MOS capacitors. Device fabrication was completed with a 450°C, H_2 anneal.

The control wafer and unannealed portions of the device wafers had a moderately high fixed-charge density of about $2.3 \times 10^{11}\,cm^{-2}$, as expected from the processing employed. The magnitude of this fixed charge decreased with increasing laser power, as seen in Fig. 2, to a minimum value of about $5 \times 10^{10}\,cm^{-2}$ at the highest laser powers on two different wafers. (Different laser powers were used on different regions of each wafer. The reflection from the oxide-coated wafer and consequently the effectiveness of a given laser power depends, of course, on the thickness of the oxide.) Bias-temperature stress showed that the decrease in fixed-charge density is not related to mobile ions. The shape of the $C-V$ curve indicated a moderate fast-state density. A density of approximately $(5.0 \pm 1.3) \times 10^{10}\,cm^{-2}$ was seen in the unannealed regions, while the fast-state density was $(7.6 \pm 1.7) \times 10^{10}\,cm^{-2}$ in the laser-annealed regions. Thus, from this experiment we see that laser annealing can reduce the magnitude of an initially high fixed-charge density at the silicon-dioxide/single-crystal-silicon interface

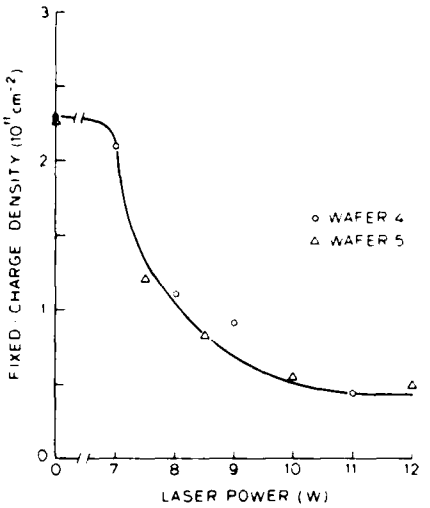

Fig. 2. Fixed-charge density at a silicon-dioxide/single-crystal-silicon interface as a function of laser power.

beneath a thermally grown oxide while only slightly increasing the fast-state density. This result is consistent with the decrease of the fixed-charge density beneath a layer of deposited oxide seen after laser annealing[3].

The third experimental structure investigated (Fig. 1c) contained a layer of low-pressure CVD silicon nitride deposited directly on silicon and was designed to see if laser annealing would improve the normally poor characteristics of a silicon-nitride/single-crystal-silicon interface. After the 0.1 μm-thick layer of silicon nitride was deposited, the wafers were laser annealed. No high-temperature thermal anneal was used before laser annealing since laser parameters for structures with polysilicon deposited on nitride are generally less critical than those with polysilicon deposited on oxide. After laser annealing at powers ranging from 3 to 10 W, with a focusing lens of 135 mm focal length, aluminum was deposited, defined, and annealed in H_2 at 450°C, as described above.

Unlike the case of silicon dioxide, these devices showed a very high fixed-charge density for all laser powers used, with an average of $(1.1 \pm 0.1) \times 10^{12}\,cm^{-2}$ before any bias-temperature stress. A negative bias-temperature stress changed the C-V characteristics very little, with only a slight negative change in the flatband voltage (~ -0.06 V). A subsequent positive bias-temperature stress ($1 \times 10^6\,V\,cm^{-1}$ at 300°C) significantly increased the flatband voltage, with the amount of the change increasing with increasing laser power (Fig. 3). The direction of these shifts is opposite to that expected from mobile ion contanimation and is consistent with the injection of electrons into the insulator by a positive stress. These electrons may easily pass through a thin, residual oxide layer between the silicon and the silicon nitride to remain at the oxide/nitride interface or to be distributed into the silicon nitride. We might speculate that the increasing flatband-voltage change with increasing laser power results from the laser annealing disrupting the thin, residual oxide layer, making electron in-

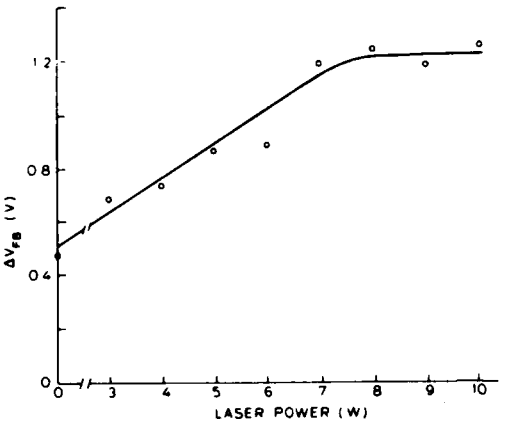

Fig. 3. Flatband-voltage change caused by positive bias-temperature stress as a function of laser power for a laser-annealed, silicon-nitride capacitor.

jection into the insulator or trapping there easier. The shape of the C–V curves indicates a fast-state density of approximately 1.0×10^{11} cm^{-2} in both the laser-annealed and unannealed regions. Thus, observations on this structure suggest that laser annealing does not significantly improve the quality of a silicon/silicon-nitride interface.

The results of this series of experiments allow the following three conclusions to be drawn: (1) Laser melting and recrystallization of a polysilicon gate above a thermal oxide does not appreciably increase the interface charges at the underlying silicon-dioxide/single-crystal-silicon interface. (2) Laser annealing of a thermally grown silicon-dioxide layer significantly reduces an initially high fixed-charge density. (3) Similar annealing of a silicon-nitride-covered silicon wafer does not markedly reduce the fixed-charge density but may make electron injection into or trapping in the insulators easier.

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Thin film MOSFET's fabricated in laser-annealed polycrystalline silicon

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Both depletion- and enhancement-mode MOSFET's have been fabricated with the active transistor channels in laser-annealed polycrystalline-silicon films. A dose of 3×10^{12} $^{31}P/cm^2$ was implanted at 100 keV into 0.5-μm-thick poly-silicon films for the depletion-mode device, and a dose of 3×10^{11} $^{11}B/cm^2$ was used for the enhancement-mode device. The transistors fabricated in the poly-silicon films show electrical characteristics comparable to those of devices in single-crystal silicon. In the depletion-mode device, an electron mobility of ~450 $cm^2/Vsec$ was obtained, and approximately 80% of the phosphorus was electrically active. The surface mobility of electrons was about 340 cm^2/V sec in the enhancement-mode device, and a threshold voltage of approximately 2.5 V was obtained.

PACS numbers: 73.60.Fw, 83.30.Tv, 68.55. + w

Polycrystalline silicon formed by chemical vapor deposition is commonly used in integrated circuits for interconnections, gate electrodes, and resistors. The material is easy to prepare and is compatible with monolithic silicon integrated circuit technology; however, the relatively small grain size tends to limit its application since the grain boundaries usually affect the transport properties. For example, *p-n* junction diodes in poly-silicon exhibit minority-carrier lifetimes of the order of 20 psec. [1] MOSFET's fabricated to date on thin films of poly-silicon have also exhibited poor transconductance. [2]

It has been recently demonstrated that the grain size of poly-silicon can be increased dramatically by annealing the material with a scanning argon cw laser. [3] With 0.5-μm-thick poly-silicon films formed by chemical vapor deposition on a substrate of 1000 Å Si_3N_4 deposited on a single-crystal silicon wafer, TEM observation showed a grain size of $\sim2\times30$ μm after laser annealing, while the original grain size was ~500 Å. The grains extended through the entire thickness of the film and were found to be defect free. With a boron implantation dose of $5\times10^{14}/cm^2$, the implanted impurities were found to be 100% activated, and the Hall mobility was essentially that of single-crystal material.

These results suggested that laser-annealed poly-silicon may be useful as an active device material. MOS field-effect transistors were chosen as a suitable experimental vehicle for the study since they utilize majority-carrier properties and are important in MOS integrated circuits. Channel lengths of, or smaller than, the grain size in laser-annealed poly-silicon may be expected to yield device performance comparable to that of devices fabricated in single-crystal silicon, whereas the properties of the grain boundaries have been found to dominate the device behavior in fine-grained poly-silicon. [2]

The poly-silicon samples used were 5500 Å thick, and were prepared by low-pressure chemical vapor deposition (LPCVD). The substrates were single-crystal silicon onto which a 1000-Å layer of Si_3N_4 had been deposited. Phosphorus was implanted at an energy of 100 keV with a dose of $3\times10^{12}/cm^2$ to form the channel for the depletion-mode devices. Boron was implanted at an energy of 100 keV with a dose of $3\times10^{11}/cm^2$ for the enhancement-mode devices. The wafers were then annealed by an argon cw scanning laser so that long grains were formed. The annealing conditions were similar to those in Ref. 3.

The subsequent processing steps for the depletion-mode devices were as follows: First, 5000 Å of low-temperature CVD oxide was deposited and densified at 900 °C. Source and drain regions were then photolithographically defined. Phosphorus was added to these regions by a 950 °C 30-min $POCl_3$ predeposition, followed by a 900 °C 10-min dry-O_2 drive-in. An additional 2000 Å of oxide was then deposited to cover the n^+ source and drain regions. Isolation photolithography defined mesas for the depletion-mode devices, and the oxide and poly-silicon were etched to isolate each transistor. The deposited oxides were then etched away, and 5000 Å of oxide was deposited to ensure that steps formed by the isolation pattern were covered during subsequent processing. The gate area was photolithographically defined, and the oxide was etched. A 1000-Å gate oxide was grown at 1100 °C in dry O_2 for 42 min, and contact holes

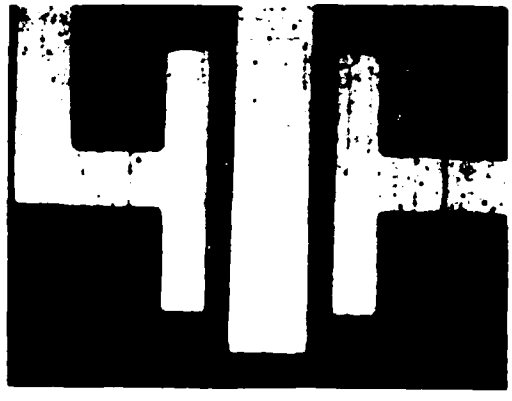

FIG. 1. Photograph of a depletion-mode device (channel length = 50 μm; magnification = 220×).

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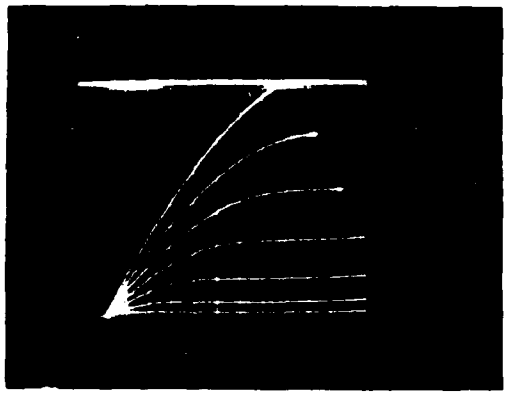
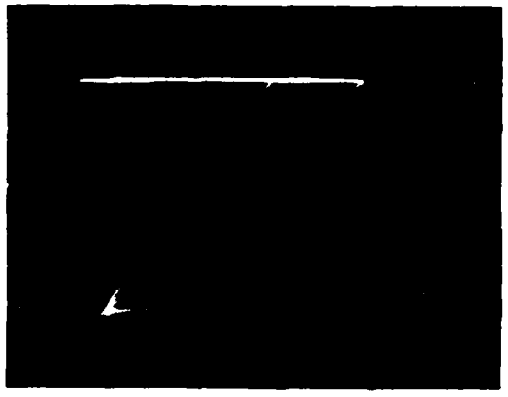


(a)



(b)

FIG. 2. (a) Source-drain I-V characteristics for a depletion-mode device ($V_G = 0$ to -12 V). (b) Source-drain I-V characteristics for an enhancement-mode device ($V_G = 0$ to 7 V).

were etched above the source and drain regions. Aluminum metallization was formed by e-beam deposition. The aluminum was defined and etched to form the gate electrode and connections to the other electrodes. The devices were then annealed in N_2 at 450 °C for 30 min. A photograph of the final depletion-mode device structure is shown in Fig. 1. Fabrication of the enhancement-mode devices was similar except that steps related to the mesa formation were omitted since no isolation is required between devices.

Devices with channel lengths of 10, 20, and 50 μm were fabricated; the channel widths were 250 μm for the depletion-mode devices and 270 μm for the enhancement-mode devices. Since the grains formed by laser annealing tend to align themselves with the laser scan directions, the channels were fabricated both parallel and perpendicular to the laser scan direction.

The source-drain I-V characteristics of both the enhancement- and depletion-mode devices are shown in Fig. 2. Since the current in a depletion-mode transistor flows through the entire thickness of the conducting layer, film properties can be calculated from the transconductance and drain current. In the linear region the transconductance is as follows[4]:

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu C_{ox} \frac{W}{L} (V_D - V_S).$$

From the transistor channel geometry ($L = 50\,\mu$m, $W = 250\,\mu$m), the mobility is calculated to be 450 cm^2/V-sec, compared to a mobility of 750 cm^2/V sec in single crystal silicon at a dopant concentration of 6×10^{16} cm^{-3}, corresponding to the dose implanted into the poly-silicon film. (Because the film melted during laser annealing,[3] the phosphorus can be assumed to be uniformly distributed through the thickness of the film, and, as will be shown below, most of the implanted phosphorus contributed electrically active carriers. Therefore, the entire implanted dose can be used to calculate the average dopant concentration.) Because of the high oxidation temperature, the gate-oxide thickness can be assumed to be the same as that on single-crystal silicon (1000 Å).

One can also calculate the carrier concentration in the channel from the geometry of the device and the flatband voltage,[4]

$$V_{FB} = \phi_{MS} - \frac{Q_{ss}}{C_{ox}} - \frac{1}{C_{ox}} \int_0^x \rho(x)\, dx.$$

If most of the dopant in the poly-silicon is active, ϕ_{MS} is equal to that of single-crystal silicon (-0.21 V), and the gate-oxide thickness may again be assumed to be the same as that on single-crystal silicon. Since Q_{ss}/q was found to be 1×10^{11} cm^{-2} on enhancement-mode transistors fabricated on (100)-oriented single-crystal wafers in the present experiment, and a value three times as high would be expected on (111)-oriented silicon, $Q_{ss}/q = 2 \times 10^{11}$ cm^{-2} is used in the calculation of V_{FB} for the poly-silicon device to account for the random orientation of the crystallites. Assuming the third term to be negligible, a flatband voltage of -1.1 V is obtained with an uncertainty of ± 0.5 V because of possible deviations of Q_{ss}/q from the value used.

From the resistance at $V_G = V_{FB} = -1.1$ V, an average carrier concentration of 5×10^{16} cm^{-3} can be calculated from

$$N = L/q\mu WdR,$$

where $d = 0.5\,\mu$m is the thickness of the film. Since this value is comparable to the average dopant concentration of 6×10^{16} cm^{-3} added by ion implantation, it is seen that a high percentage of the dopant is electrically active, and little has been lost during processing. The film properties observed in these laser-annealed poly-silicon films are compared to the bulk properties of single-crystal silicon and also to those of fine-grained poly-silicon at a dopant concentration of 6×10^{16} cm^{-3} in Table I.

For the enhancement-mode device the field-effect mo-

TABLE I. Electrical properties of poly-silicon and single-crystal silicon at an average dopant concentration of 6×10^{16} cm^{-3}

	Laser-annealed poly-silicon	Single-crystal silicon	Fine-grained poly-silicon[a]
Carrier conc. (cm^{-3})	5×10^{16}	6×10^{16}	$\sim 1 \times 10^{15}$
Mobility (cm^2/V sec)	450	750	~60
Resistivity (Ω cm)	0.28	0.14	$\sim 1 \times 10^{3}$

[a] J. Y. W. Seto, J. Appl. Phys. 46, 5247 (1975), for holes.

bility is similarly calculated from the source-drain characteristics in the linear region and the device geometry ($L = 50\ \mu$m, $W = 270\ \mu$m) to be 340 cm^2/V sec. This value may be compared to the value of 630 cm^2/V sec expected for the field-effect mobility in single-crystal silicon of the same dopant concentration (50% of the bulk mobility [6]).

The threshold voltage (defined to be the gate voltage which induces a drain current of 1μA) is measured to be + 2.5 V. Again, assuming $Q_{ss}/q = 2\times10^{11}$ cm^{-2}, the threshold voltage is calculated to be − 0.2 V in the absence of defect levels in the poly-silicon. The difference between the measured and calculated threshold voltages may be attributed to the charging of defect levels before the surface can be inverted, as well as to uncertainties in the value of Q_{ss}/q used in the calculations. This difference represents a significant improvement over previous poly-silicon MOSFET's, where differences about one order of magnitude larger were observed. [2]

Both depletion- and enhancement-mode MOSFET's have been fabricated with the active transistor channels in films of laser-annealed poly-silicon. The devices showed electrical characteristics reasonably close to those expected in transistors constructed in single-crystal silicon. These results suggest that high-quality integrated circuits can be fabricated using laser-annealed poly-silicon as the semiconductor layer either in addition to, or in place of, bulk single-crystal silicon.

The authors are indebted to ARPA (Contract MDA 903-78-C-0290) and to Dr. R. Reynolds for the support of this work.

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from the results of the 60 W electron-beam-annealed diode only in having a slightly lower intercept voltage of 0·55 V. This intercept value for the thermally annealed diode is close to that expected for the built-in potential of a high-doping-ratio p^+-n junction.[8] The higher values of intercept observed for the electron-beam-annealed diodes (0·8–0·65 V) are probably associated with the residual damage present in the junction region from partial annealing.

The characteristics of 60 W scanning-electron-beam-annealed junctions compare favourably with those published for continuous-laser-annealed diodes. In the forward-bias region, the laser annealed diodes show nonlinear behaviour[5] or large variations in the diode-ideality factor,[4] whereas the electron-beam-annealed diodes approximate to the ideal over four decades of forward current. The inferior reverse characteristics[4,5] of laser-annealed diodes have been attributed to residual damage created by the annealing process at the Si/SiO_2 interface. In contrast to these results, leakage measurements on electron-beam-annealed diodes imply that interfacial or peripheral diode damage is minimal.

At 30 keV beam potential, the range of electrons in Si is 6·3 μm, with maximum energy loss occurring at 2·5 μm. Thus for all the diode structures studied in the present work, the maximum energy loss will have occurred below the combined junction and zero-bias-depletion depth. The observation of uniform doping profiles at the depth of maximum energy loss indicates that the beam irradiation necessary to induce solid-phase epitaxial regrowth of the shallower-implant damage region does not perturb the substrate material. Further, the present diode measurements suggest that the most likely location of residual damage is within the p^+ or junction regions. T.E.M. and s.e.m. studies are currently in progress to investigate this possibility. Further scanning-electron-beam-annealing experiments will be conducted at lower beam potentials to explore the effects of matching the maximum energy dissipation with the ion-implant damage profile.

The results of the present work show that diodes with characteristics close to those of identical thermally annealed structures can be fabricated using scanning-electron-beam annealing. Diode characteristics produced by scanning-electron-beam annealing are dependent on electron-beam parameters, especially beam power and exposure, and it has been shown that for a 100 keV B-implant, optimum annealing conditions are close to the 60 W (30 keV, 2 mA) results reported.

It is foreseen that scanning-electron-beam annealing can be developed for the practical formation of device junctions and for localised thermal modification of other semiconductor-device material layers.

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SILICON-ON-INSULATOR M.O.S.F.E.T.S FABRICATED ON LASER-ANNEALED POLYSILICON ON SiO_2

Indexing term: Insulated-gate field-effect transistor

N-channel-enhancement and light-depletion-mode m.o.s.f.e.t.s have been fabricated on laser-annealed 0·5 μm polysilicon films, deposited on 1 μm of SiO_2 grown on single-crystal silicon substrates. Threshold voltages of 0·35–0·45 V and −0·5 –0·7 V and surface mobilities of 170 cm^2/Vs and 215 cm^2/Vs were obtained on the enhancement and depletion devices, respectively. These results compare favourably with values realised in silicon-on-sapphire (s.o.s.) and bulk *N*-m.o.s. devices. In addition, the measured source-drain leakage currents match the best reported values for s.o.s. devices.

The fabrication of enhancement- and depletion mode m.o.s.f.e.t.s in laser-recrystallised polysilicon films has been reported in recent literature.[1] The devices described were constructed on a polysilicon film 5500 Å thick. The film was grown by low-pressure chemical vapour deposition (l.p.c.v.d.) onto a layer of Si_3N_4 1000 Å thick that had been previously deposited on ⟨100⟩ single-crystal silicon. From the device performances, the laser-annealed material showed electrical properties far superior to those of as-deposited material, and comparable to those of single-crystal silicon. However, the thin nitride layer used presented problems of isolation from the substrate, nor was it an ideal choice as an insulating layer because of surface states at the nitride-silicon interface. In addition the devices fabricated had larger dimensions (of 50 μm, 20 μm and 10 μm), and they exhibited substantial source-drain leakage currents in the 10 μm-channel-length devices.

These problems lead to the question of whether a thick oxide layer is a better choice as an insulating material. It is also of interest to determine whether the laser-annealed material is useful for device fabrication with geometries that are more typical of current technology. In this communication, results are presented for silicon-on-insulator m.o.s.f.e.t.s fabricated on laser-annealed 0·5 μm polysilicon films deposited on an amorphous film of silicon dioxide grown on single-crystal silicon substrates.

The samples used in this study consist of 500 nm-thick undoped polysilicon films deposited on 1 μm of SiO_2 grown on *p*-type ⟨100⟩ single-crystal silicon substrates having a resis-

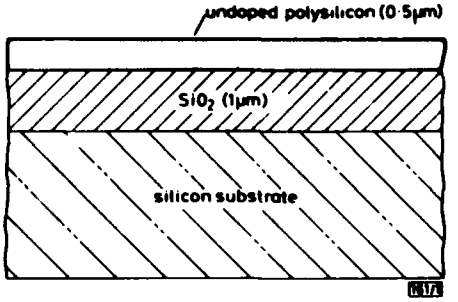

Fig. 1 *Cross-section of polysilicon/SiO_2/Si substrate samples prepared for laser annealing study*

tivity of 6-8 Ωcm (Fig. 1). The SiO_2 layer was grown by steam oxidation at 1000°C, and the polysilicon was deposited undoped onto the silicon dioxide by l.p.c.v.d.

The wafers were then thermally annealed at 1100°C in flowing N_2 for one hour. This treatment has been found to improve the surface quality of polysilicon films deposited on SiO_2 during subsequent laser anneal. Without the thermal anneal, severe etching of the polysilicon surface occurs during the laser-initiated melting and regrowth of the polysilicon that leads to the formation of long grains. For the laser anneal, a c.w. Ar^+ laser (Spectra Physics Model 171-09) was used in a scanning system previously reported for laser-annealing experiments on polysilicon.[2] A lens of focal length 136 mm was used resulting in a spot size of ≈ 40 μm. The scan rate was 12 cm/s, and the step size was 18 μm. A sample holder temperature of 350°C was used. The laser power was chosen such that long grains were observed under a Nomarski interference microscope, yet without etching of the wafer surface, and differed from 10 W to 12 W with various wafers. The long grains had been previously established to be of dimensions ≈ 2 μm × 30 μm,[2] and were of mixed crystal orientations.

After laser annealing, the wafers were processed to form *N*-channel m.o.s.f.e.t.s using a previously established high-density (gate oxide = 35–40 nm) process. The sequence of steps was as follows. The laser-annealed polysilicon was first patterned to define silicon islands in a manner similar to the silicon-island-patterning step for silicon-on-sapphire (s.o.s.) devices.[3] The patterning was accomplished with plasma etching. Next, a 35–40 nm gate oxide was grown at 1000°C using 5% HCl in O_2. This step was followed by a photolithographic resist patterning step, to allow a threshold voltage-adjustment implant to be made into selected devices. A boron implant at an energy of 60 keV and a dose of 5×10^{11} cm^{-2} was used to form enhancement devices. In this way, devices could be fabricated and evaluated on both undoped and lightly doped (using implanted boron) silicon. Following the implantation, a 500 nm-thick undoped polysilicon layer was deposited over the gate oxide using l.p.c.v.d. The polysilicon was heavily doped to N^+ by phosphorus-ion implantation, and annealed. The polysilicon was then patterned, using plasma etching, to form the gate electrode and its connections. The gate oxide over the source and drain regions was also plasma-etched, and an arsenic-ion implantation was performed at an energy of 120 keV and a dose of 1×10^{16} cm^{-3}, to form the source and drain junctions. This implant was then annealed at 1000°C for 30 min in an oxygen/nitrogen ambient. The final step was a 30 min sinter in H_2 at 450°C for minimising the surface state density at the SiO_2-Si interface.

Enhancement-mode and depletion-mode transistors having W/L ratios of 25/5, 25/10 and 25/25 (μm/μm) were fabricated on both annealed and unannealed areas of the wafers to provide a direct comparison of device type and annealed against unannealed polysilicon on the same wafer.

The I/V characteristics of enhancement (boron-implanted) and depletion (undoped polysilicon) devices, fabricated on laser-annealed areas, are shown in Fig. 2. The threshold voltages (V_T) determined from measurements of $\sqrt{I_{DS}}$ against V_G were 0·35–0·45 V for the enhancement devices, and −0·5 to −0·7 V for the depletion devices. In the unannealed areas of the wafer, the measured threshold voltages of the polysilicon transistors ranged from 7 to 10 V, with little if any difference between implanted and unimplanted devices. The mobilities were determined from the measured slope of the drain-source current (I_{DS}) against gate voltage (V_G) curves at low drain voltage ($V_D = 0{\cdot}1$ V) using the well known expression

$$g_m = \mu C_0 \frac{W}{L} V_D \tag{1}$$

where μ is the surface mobility, and C_0 is the gate-oxide capacitance per unit area. The measured surface mobilities were 170 and 215 cm^2/Vs, respectively, for the *N*-channel enhancement and depletion devices. These values compare favourably with 400–500 cm^2/Vs and 600–650 cm^2/Vs which are obtained in present *N*-channel s.o.s. devices (using 0·5 μm silicon layers) and bulk *N*-m.o.s. devices, respectively. The measured surface mobilities on polysilicon devices (areas of wafer which did not receive laser-annealing) ranged from 23–29 cm^2/Vs, which is in agreement with previous reported results.[4]

Assuming the metal-semiconductor work-function difference ϕ_{MS} to be −0·8 to −0·9 V for a heavily doped N^+ silicon gate, and assuming the fixed charge at the SiO_2-Si interface to be $Q_{ss}/q \approx 2{\cdot}6 \times 10^{10}$ cm^{-2} (typical of the process used to fabricate the devices in this study), then from the measured V_T of −0·5 to −0·7 V, a value of 10^{12}-10^{13} cm^{-3} is inferred for the average doping level of the undoped laser-annealed polysilicon, using the following equation for the threshold voltage:[5]

$$V_T = \phi_{MS} + 2\phi_F - \frac{(Q_B + Q_{SS})}{C_0} \tag{2}$$

where

$$Q_B = -qN_A t_{Si}$$

In this equation, ϕ_F is the Fermi level in the silicon film, N_A is the average doping in the film and t_{Si} is the silicon-film thickness. The value of 10^{12}–10^{13} cm^{-3} for the average doping of the undoped polysilicon is consistent with measured resistances of load resistors fabricated on undoped polysilicon deposited by the same process.

Eqn. 2 can also be applied to determine the average carrier concentration in the silicon film for the enhancement devices. Using $\phi_{MS} = -0{\cdot}9$ V, $Q_{SS}/q = 4 \times 10^{10}$ cm^{-2}, and the measured V_T value of +0·4 V, a concentration of 8×10^{15} cm^{-3} is obtained. This is in good agreement with the average value of 1×10^{16} cm^{-3} calculated from the boron-implantation dose and energy, when account is taken of partial diffusion of boron into the SiO_2 in subsequent processing. A more accurate prediction of the enhancement device threshold voltage, based on the implantation and subsequent process conditions, can be made with the aid of the SUPREM process modelling programme.[6] For the ion implantation and fabrication conditions (temperatures and times) described earlier, SUPREM predicts a threshold voltage of 0·38 V. Also, the final

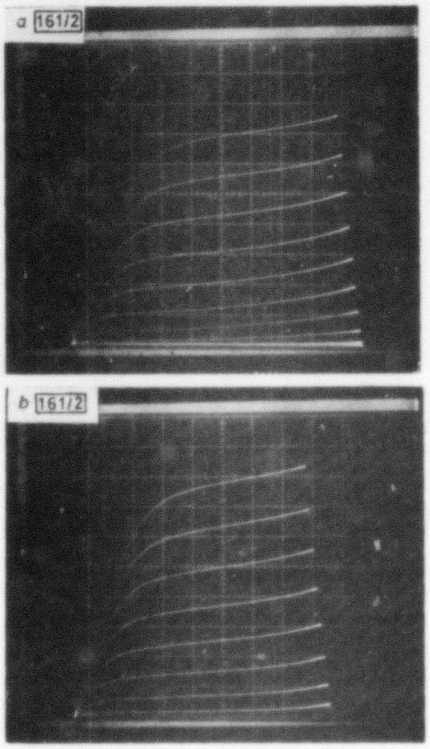

Fig. 2 *I/V characteristics of m.o.s.f.e.t.s with $W = 25$ μm and $L = 5$ μm*
The scales in both photographs are: 100 μA per vertical division, 1 V per horizontal division, 0·5 V per step, and g_m per division = 200 μS
Enhancement mode (boron implant), $V_G = 0{\cdot}5$ V
Depletion mode (undoped), $V_G = 0{\cdot}3{\cdot}5$ V

calculated boron profile drops off rapidly beyond 300 nm and is down to 5×10^{13} cm^{-3} at 500 nm. Therefore, for the 500 nm silicon film on SiO_2, the SUPREM prediction is expected to be quite valid, since a negligible amount of diffusion of boron across the underlying SiO_2-Si interface is involved.

The leakage current between the source and drain in the off condition was examined, in view of the difficulty in achieving low leakage in s.o.s. devices. With the gate and source grounded and 5 V on the drain, the measured source-drain leakage currents were 25, 50, and 160 pA for gate lengths of 25, 10 and 5 μm, respectively. All devices had channel widths of 25 μm. These results correspond to leakages of 1·6 pA per micrometre of channel width, and match the best reported values for s.o.s.

In conclusion, enhancement- and light-depletion-mode m.o.s.f.e.t.s have been fabricated on laser-annealed, 0·5 μm polysilicon films on 1 μm of SiO_2 grown on single-crystal silicon substrates. These devices are similar in structure to silicon-on-sapphire (s.o.s.) devices, and exhibit reasonably good electrical characteristics. These results for transistors fabricated on silicon dioxide grown on silicon substrates indicate the distinct possibility of fabricating silicon-on-insulator integrated circuits, with lower cost than is possible for silicon-on-sapphire, in view of the higher cost of sapphire substrates. In addition, because an SiO_2-Si interface replaces the sapphire-silicon interface, there also exists the possibility of achieving improved device characteristics, in particular at very high densities on thinner silicon films.

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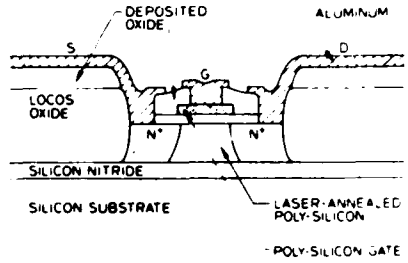

Fig. 1. Schematic representation of transistor cross section showing complete dielectric isolation formed by LOCOS oxide and insulator under the laser-annealed polysilicon.

A Monolithic Integrated Circuit Fabricated in Laser-Annealed Polysilicon

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Abstract—An integrated-circuit (IC) fabrication process has been used to construct small-geometry MOS transistors and a ring oscillator with the active transistor channels in a thin layer of laser-annealed polysilicon. Both enhancement-mode and depletion-mode n-channel, silicon-gate transistors have been fabricated with dimensions compatible with high-performance MOS technology (gate lengths as short as 3 μm). A modified LOCOS process was used to fabricate the devices so that each transistor was contained within a pocket of silicon completely isolated from adjacent elements by dielectrics. The transistors were well behaved, with mobilities approaching those in single-crystal silicon, reasonably abrupt subthreshold characteristics, and low leakage current. An operating, nine-stage ring oscillator was also fabricated, and its behavior suggests the approach for further optimization. The technology offers the possibility of high-performance IC's on potentially inexpensive substrates, as well as the possibility of additional levels of devices on monolithic silicon IC's.

INTRODUCTION

A recent report of the fabrication of MOS devices with their active channels in a layer of laser-annealed polysilicon opens the possibility of fabricating high-performance integrated circuits (IC's) in thin layers of polysilicon [1]. Use of such a layer on potentially inexpensive insulating substrates would result in low-cost large arrays, while the fabrication of devices in a polysilicon layer above and insulated from a conventional, single-crystal silicon IC would offer the opportunity for almost doubling IC component density, as well as the possibility of novel vertical structures.

The first report [1] described the fabrication of large-geometry, aluminum-gate MOS transistors. The present brief describes the fabrication of silicon-gate MOS transistors of dimensions compatible with high-performance MOS IC technology; both enhancement-mode and depletion-mode transistors were fabricated with an IC process. A functioning, integrated ring oscillator containing both enhancement-mode driver transistors and depletion-mode load elements was constructed; the performance of this circuit suggests the approach for process optimization.

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DEVICE FABRICATION

The 0.5-μm-thick layer of polysilicon to be laser annealed was formed by LPCVD on top of a 1000-Å-thick layer of insulating silicon nitride deposited on a single-crystal silicon wafer. Previous experience has indicated that the laser annealing proceeds most readily above silicon nitride [2], although recent work has achieved similar annealing above silicon dioxide [3], which would be preferred for optimal device behavior. After the polysilicon was implanted with boron (doses of 2×10^{11} or 3×10^{11} cm^{-2} at 100 keV), it was laser annealed at Stanford University with a scanned argon laser as described previously [2]. Laser annealing melted and recrystallized the fine-grain polysilicon to form large-grained material [1].

To remain compatible with standard monolithic silicon IC technology as much as possible, subsequent processing at Hewlett-Packard followed LOCOS [4] technology with suitable modifications to account for the structure of the polysilicon. A layer of silicon nitride was deposited above a thin stress-relief oxide and patterned to retain the nitride in the active device regions. Projection alignment was used for all photomasking operations. The exposed polysilicon was then oxidized until the oxide reached the insulator beneath the polysilicon so that each device island of polysilicon was completely isolated from adjacent islands and from the substrate by dielectrics, as shown in Fig. 1. Completion of the oxidation process is easily determined since a thin layer of unoxidized polysilicon is readily observable when it is present between the insulators above and below. (Alternatively, the polysilicon between device islands could be removed by etching.) After the remaining nitride was removed, the gate oxide was grown at 1000°C in a TCE/dry O_2 ambient. The oxide grown on the polysilicon under these conditions was found by an ultraviolet interference technique [5] to be approximately 6 percent thicker than the 1000-Å-thick oxide simultaneously grown on (100)-oriented, single-crystal silicon. No significant difference in oxide thickness was found between the laser-annealed and the unannealed regions. After the gate oxidation, the depletion-mode load transistors were selectively implanted with phosphorus while the enhancement-mode transistors were protected with photoresist. Doses of 7×10^{11} and 1.4×10^{12} cm^{-2} were implanted at 150 keV so that the phosphorus penetrated through the gate oxide.

The gate polysilicon was then deposited by LPCVD, doped by a $POCl_3$ predeposition, and defined by chemical etching. Even though the surface of the underlying laser-annealed polysilicon is rougher than a polished single-crystal substrate, no difficulties were encountered in defining lengths of 3 μm in the gate polysilicon. The source and drain regions were then implanted with phosphorus, and the entire structure was protected with a low-temperature deposited oxide to minimize

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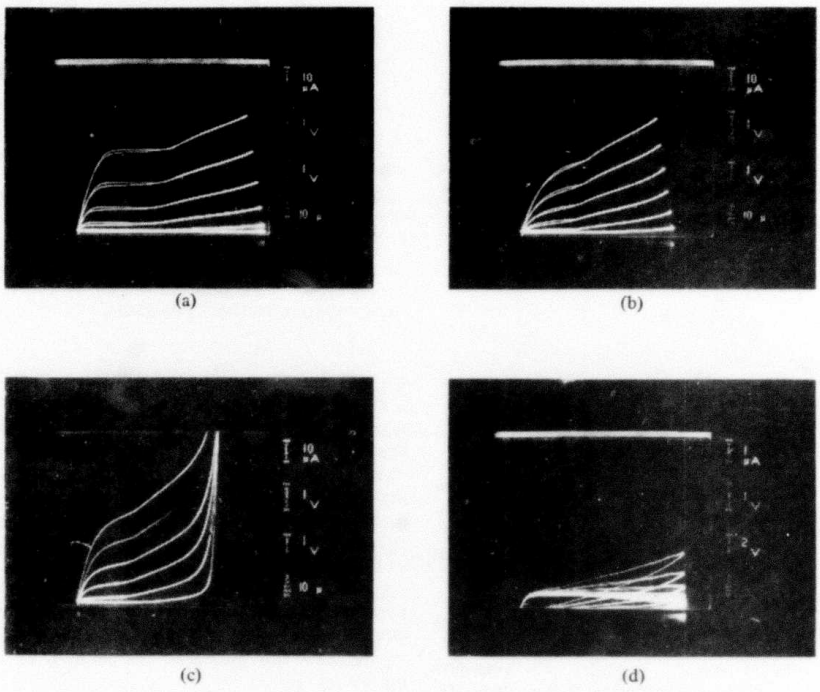

Fig. 2. Source–drain characteristics of transistors fabricated in polysilicon. (a) $L = W = 20$ μm in laser-annealed region; 5 1-V-gate steps; (b) $L = 4$ μm, $W = 5$ μm in annealed region; 5 1-V-gate steps; (c) $L = 3$ μm, $W = 4$ μm in annealed region; 5 1-V-gate steps; (d) $L = 4$ μm, $W = 5$ μm in unannealed region; 10 2-V-gate steps (note different current scale).

further high-temperature heat treatment. After an anneal to activate the source and drain dopant atoms and to improve the source and drain junction characteristics, contact windows were opened, and 1 μm of conventional aluminum–silicon alloy was deposited and defined. A hydrogen anneal completed the fabrication process.

Capacitance–voltage measurements between large-area diffusions and the underlying substrate indicate that the source–drain dopant reached the underlying dielectric since the maximum capacitance corresponded to that of the deposited nitride.

Transistor Behavior

Both large-area and small-geometry transistors were tested to determine the threshold voltages and other transistor parameters. On a curve tracer the transistors appeared well-behaved, with well-saturated square-law characteristics seen on the large-geometry transistors (Fig. 2(a)) at moderate drain voltages. At higher drain voltages, the current began increasing with increasing drain voltage. This so-called "kink effect" has been observed in silicon-on-sapphire transistors and is attributed to a forward bias appearing on the floating film beneath the channel depletion region [6]. At these drain voltages, weak avalanching near the drain end of the transistor creates electron–hole pairs. The holes flow to the neutral region of the p-type film, causing this floating region to become forward biased, with a consequent decrease in effective channel-to-film voltage and increase in channel current. The kink effect was not seen in devices simultaneously fabricated on single-crystal control wafers.

For shorter gate lengths, short-channel effects similar to those seen on the single-crystal control wafers prevented obtaining a well-saturated region. The onset of the kink effect was still easily observed, however (Fig. 2(b) and (c)). Functional transistors were obtained with channel lengths as short as 3 μm (mask dimension) (Fig. 2(c)), but the results reported here for small-geometry transistors were measured on devices with mask dimensions $L = 4$ μm and $W = 5$ μm since this gate length is used in the ring oscillator. (The final transistor channel was measured optically to be approximately 4 μm square.)

More detailed measurements indicated some source–drain leakage which could be eliminated by applying a small voltage to the single-crystal substrate to accumulate the bottom surface of the silicon film. This leakage probably occurs when the depleted silicon surface intersects the underlying nitride film and is probably caused by generation through the many surface states expected at this interface. It should be eliminated by the deposition of the active polysilicon layer on silicon dioxide, rather than on silicon nitride. In a previous study on structures formed by electrochemical etching, states at the silicon–silicon dioxide interface beneath a thin film of single-crystal silicon were found to be easily annealed, providing ideal interface characteristics [7]. The results described below were obtained with a negative substrate bias applied to accumulate the bottom surface of the polysilicon film unless otherwise noted. The transistor parameters were independent of the magnitude of this bias from at least −2 to −6 V.

With the substrate bias applied, the enhancement-mode threshold voltages measured at 1 μA in the saturation region ($V_D = 2.5$ V) were 1.4 V on large-area square transistors and 1.1 V on small-geometry devices ($L = 4$ μm, $W = 5$ μm). For comparison, no significant conduction was observed in similar transistors fabricated in areas of polysilicon which had not been laser annealed (Fig. 2(d)), even with as much as 20 V applied to the gate. The depletion-mode implant of 1.4×10^{12} cm^{-2} shifted the threshold voltage of the large-area laser-

annealed transistors by −2.5 V. The current flowing in the depletion-mode transistors was measured at zero gate voltage on the large-area transistors to be 3.6 μA in the saturation region (V_D = 2.5 V). On small-geometry transistors, the average current was 27 μA, with considerable variation from device to device.

The subthreshold current was characterized by an inverse slope of approximately 200 mV/decade of current on both the enhancement-mode and depletion-mode transistors. Similar subthreshold measurements on the unannealed portion of the polysilicon film indicate a subthreshold slope of 2.4 V/decade over a limited range of drain current, again demonstrating the dramatic changes caused by the laser recrystallization. The subthreshold slope on the single-crystal control wafer varied from 142 to 113 mV/decade as the substrate voltage was changed from 0 to −6 V. When the gate in the laser-annealed polysilicon region was biased below threshold, the substrate voltage could be used to induce transistor action at the bottom of the silicon film. The subthreshold slope in this mode of operation was approximately 530–600 mV/decade on the enhancement- and depletion-mode transistors, consistent with the assumption of a high density of surface states at the polysilicon/silicon-nitride interface. A portion of this high density will also increase the front-surface subthreshold slope when the entire film is depleted.

The channel electron mobility was calculated from the large-geometry transistors operated in the linear region to be about 270 $cm^2/V \cdot s$ for the enhancement-mode devices and 300 $cm^2/V \cdot s$ for the depletion-mode devices. These values are about an order of magnitude larger than the 20 $cm^2/V \cdot s$ observed for transistors fabricated in similarly doped, fine-grained polysilicon [8]. The large difference in device behavior appears to be correlated with obtaining the large-grained structure by melting and recrystallization since similar results were obtained for all laser powers that produced the large-grained structure. The mobility of 270 $cm^2/V \cdot s$ may be compared to that in transistors fabricated simultaneously in single-crystal control wafers, which varied from 700 to 580 $cm^2/V \cdot s$ as the substrate bias was changed from 0 to −6V.

The source–drain leakage current at V_D = 0.1 V with the gate biased below threshold was a fraction of 1 pA (typically 0.2–0.9 pA) for small-geometry transistors, while 50-μm-wide devices with L = 4 μm indicated a leakage current of 0.06 pA/μm of gate width. At 5-V drain voltage, the leakage current in the small-geometry transistors averaged 10 pA.

Ring Oscillator

The monolithic ring oscillator consisted of nine nearly identical oscillator stages and three output buffer stages. Each oscillator stage contained an enhancement-mode driver transistor with L = 4 μm and W = 9 μm and a depletion-mode load transistor with L = 8 μm and W = 4 μm (dimensions measured optically on the wafer). The output buffer contained enhancement-mode transistors with L = 4 μm and W = 9, 30, and 133 μm on successive stages, and similarly scaled depletion-mode load transistors. Both devices of each stage were contained in one dielectrically isolated silicon island since the intermediate node is common to both transistors.

The output waveform is shown in Fig. 3. Oscillations were consistently observed with a supply voltage of approximately 14–16 V. This high operating voltage resulted from the non-optimum thresholds of both the enhancement- and depletion-mode transistors. At moderate supply voltages, the voltage at the intermediate node of the ON stage was too high to fully turn off the succeeding stage. At higher supply voltages, the intermediate-node voltage of the OFF stage increased so that the enhancement-mode transistor of the following ON stage was more conductive, and the intermediate-node voltage above this transistor became low enough to turn off the next

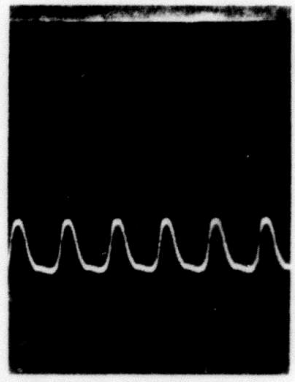

Fig. 3. Output waveform of ring oscillator; horizontal scale: 50 ns/div; vertical scale: 0.2 V/div; V_{DD} = 14 V; V_{SUB} = −6 V.

enhancement-mode transistor, allowing oscillations to occur because of the odd number of stages. The authors believe that a higher threshold voltage for the enhancement-mode transistor coupled with a lower zero-bias current for the depletion-mode transistor would decrease the required supply voltages to those commonly used for IC operation.

The period of the output signal averaged 70 ns for this nine-stage ring oscillator. Calculation of the capacitances from the device dimensions indicates that 60 percent of the 0.8-pF capacitance which must be charged to change the state of each stage is associated with the thin nitride under the polysilicon. Reducing this contribution by the use of a thick oxide or an insulating substrate would significantly reduce the overall capacitance, with a corresponding decrease of the propagation delay time. For a 1.4-μm-thick oxide under the polysilicon, the overall capacitance would be reduced to about 0.035 pF. In addition, the use of either a thick oxide or an insulating substrate beneath the polysilicon would reduce the interconnection capacitance below that of a conventional IC. An insulating substrate with a low permittivity would even decrease the capacitance below that of silicon-on-sapphire, which suffers from the high permittivity of sapphire contributing to fringing capacitance between adjacent parallel interconnection lines.

Conclusion

Small-geometry transistors and a simple monolithic circuit have been fabricated in a layer of large-grained laser-annealed polysilicon with an IC process. The transistors were well-behaved; the mobilities were much greater than those in fine-grained polysilicon and approached those in single-crystal silicon; the transistors exhibited reasonably abrupt subthreshold characteristics and low leakage current.

A functioning ring oscillator has been fabricated, showing the possibility of IC's in laser-annealed polysilicon, and its operation suggests the direction for process optimization to improve circuit performance. Calculation of the capacitances associated with the structure indicates that significant speed improvement could be achieved by the use of a thick oxide or an insulating substrate, rather than a thin nitride layer, under the active layer of polysilicon to reduce the capacitance to the substrate. Eliminating the polysilicon/silicon-nitride interface should also reduce the leakage current.

With these improvements, fabrication of IC's within a layer of laser-annealed polysilicon offers the possibility of high-performance IC's on potentially inexpensive substrates, as well as the possibility of additional levels of devices on monolithic single-crystal silicon IC's.

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Ring Oscillators Fabricated in Laser-Annealed Silicon-On-Insulator

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K.F. LEE, AND J.F. GIBBONS, FELLOW, IEEE

Abstract — **Both seven and eleven stage n-MOS ring oscillators with 6 μm channel length have been successfully fabricated in scanning, CW argon laser-annealed polycrystalline silicon islands, which are defined prior to the laser annealing step, on oxide substrates. The ring oscillators, which have a fan-out of three, have a switching delay per stage of 58 nsec and a power-delay product of about 7 pJ operating at a supply voltage (V_{DD}) of 5 volts and switching between V_{DD} and ground. The most serious difficulty encountered during circuit fabrication was the deformation of the silicon islands resulting from laser annealing with extensive laser power density.**

Results of devices fabricated in laser-annealed silicon-on-insulator (SOI) have shown that SOI can be a potential material for integrated circuit applications [1], [2], [3]. Recently, a functional nine-stage ring oscillator was successfully fabricated in laser-annealed polysilicon-on-nitride [4]. However, a 16 volt supply was needed to drive the ring oscillator. In this letter, we report our results on ring oscillators fabricated in laser-annealed silicon-on-oxide substrates that operate at a supply voltage of 5 volts.

The starting material (Figure 1) was prepared by growing a 1 μm thick layer of oxide (SiO_2) on p-type <100> single crystal silicon substrates with bulk resistivity of 6 Ω-cm. Five hundred nanometers of LPCVD undoped polysilicon were deposited on the oxide substrate at 620°C. Standard photolithographic and plasma etching techniques were utilized to define the polysilicon islands. This differs from all previous work, where the polysilicon islands are defined after the laser annealing. The samples were annealed in a nitrogen ambient at 1100°C for one hour. This thermal annealing step has been shown to improve the adhesion of the polysilicon onto the oxide substrate during laser annealing [1]. The sample was then laser annealed, using a scanning CW argon laser operating at 4W with a scan velocity of 12 cm per second and a line-to-line step-size of about 18 μm. A 135 mm focal length lens was used to focus the beam to a spot size of 40 μm. The substrate was kept at 350°C. The devices and circuits on the sample were fabricated by a standard depletion load, silicon gate n-MOS process which requires nine mask levels. A 500Å gate oxide thickness was used. Because the polysilicon islands were defined and etched prior to the laser annealing, a channel stop implant was not performed in the circuit fabrication.

We have observed that the window of beam power for proper laser annealing of the polysilicon islands is small. At the above stated laser annealing condition, the laser beam does not significantly alter the shape of the polycilicon islands. However, polysilicon islands annealed at a higher beam power resulted in rounding at the edges of the islands. Further increase in the beam power resulted in the complete loss of the original shape of the polysilicon islands, probably due to extensive melting.

There are two ring oscillator circuits on each die, a seven and an eleven stage circuit. The individual inverter stage in the ring oscillator circuits consists of a 6 μm channel length enhancement mode driver device and a deep depletion device as the load. Each stage has a fan-out of three and there is a two-stage source-follower at each output as the buffer.

A total of five dies were obtained from the laser-annealed area, which was about 1 cm^2. Among the five dies we found that both the seven and the eleven stage ring oscillators on two dies were functional and had very similar performance.

In Figure 2, the dela_ per stage and the power-delay product of an eleven stage ring oscillator is plotted as a function of the supply voltage (V_{DD}). These results were obtained for the ring oscillator operating in the large signal regime, namely, inverting between V_{DD} and ground. The minimum propagation delay obtainable was 44 nsec per stage at 10 volts V_{DD} and the minimum power-delay product for sustaining oscillation was 4.1 pJ. At 5 volts V_{DD}, the propagation delay and the power delay product are 57.5 nsec and 7 pJ, respectively.

Isolated enhancement mode devices, which have the same geometry as the driver in the ring oscillator circuit, were also characterized. A surface electron mobility of about 300 cm^2/V-sec (compared to 640 cm^2/V-sec measured in devices fabricated in bulk silicon slices), a threshold voltage of about -2 volts and a subthreshold leakage current of about 10 nA per micron channel width with −5 volts gate voltages and 5 volts supply voltage were measured. Isolated depletion mode devices having the same geometry as the load device in the ring oscillator exhibited a typical threshold voltage of −3.6 volts and a drain current of typically 196 μA at 5 volts supply and with the gate grounded. The subthreshold current decreased by about 3-1/2 decades per volt gate voltage. The shape of the subthreshold I-V characteristics and the fact

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that the leakage current did not scale with the channel width indicate that the edge-related leakage current dominates, a result not surprising since no channel stop implant was used. As a reference, the propagation delay in similar ring oscillators fabricated in bulk silicon, with a depletion width of 3 μm between the n+ region and the substrate (and thus the same n+ to substrate capacitance compared to that provided by the 1 μm thick oxide layer), and operating in the large signal mode is typically 36 nsec at 5 volt V_{DD}.

As a result of the -2 volt threshold voltage encountered in the enhancement mode device, 2 volts was applied to the source and 7 volts to the drain. The bulk substrate was grounded. The threshold of the enhancement mode devices was chosen to be 0.6 volt in the device fabrication. The unexpected shift in the threshold voltage was probably due to an accidental contamination in our laboratory which affected this and several other lots.

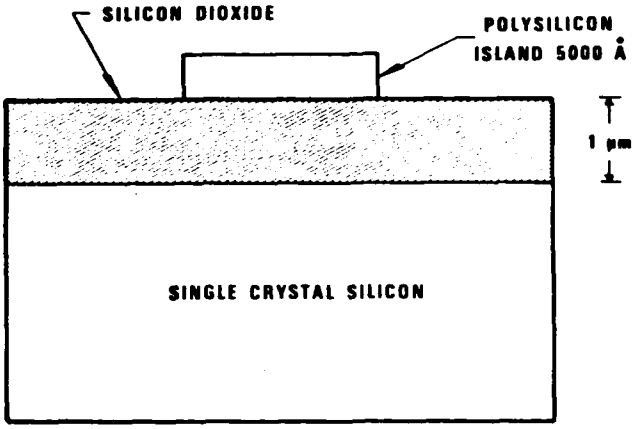

Fig. 1. Material configuration before laser annealing.

Conclusion

We have successfully fabricated and tested ring oscillator circuits in laser-annealed polysilicon islands, which are defined prior to the laser annealing, on an amorphous oxide substrate. The ring oscillator has a 57.5 nsec switching delay and a 7 pJ power-delay product at 5 volts supply voltage. A surface electron mobility of 300 cm^2/V-sec has been measured from isolated devices. The major problem encountered is the deformation of the polysilicon islands when the laser beam power is too high. This deformation causes significant difficulties in subsequent processing.

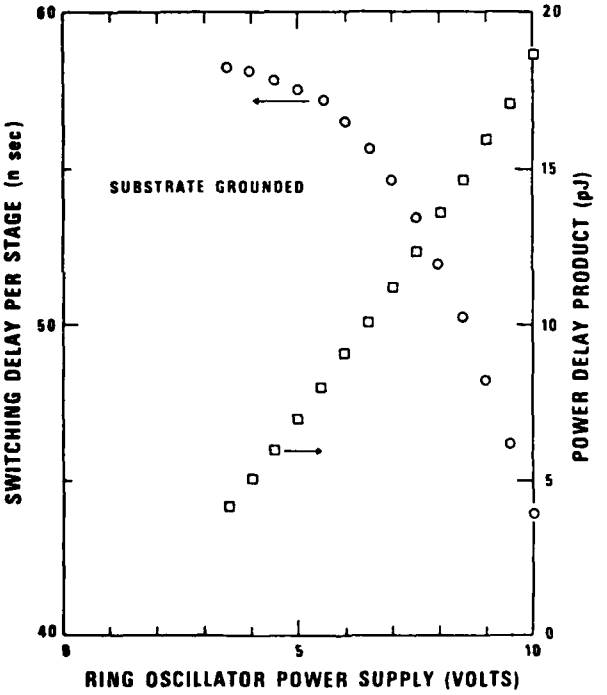

Fig. 2. Switching delay and power-delay product per stage of an eleven stage ring oscillator with the substrated grounded. The channel length of the driver transistors is 6 μm.

Acknowledgement

The authors gratefully acknowledge Dr. P.K. Chatterjee for many helpful discussions. Two of the authors (K.F. Lee and J.F. Gibbons) would like to thank ARPA (Contract No. MDA-903-78-C-0128) and Dr. R. Reynolds for continued support and interest. The other three authors (Hon-Wai Lam, A.F. Tasch, Jr., and T.C. Holloway) acknowledge ONR (Contract No. N00014-79-C-0790) and Mr. M.N. Yoder for support and interest in this research.

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MICROMETRE-GATE M.E.S.F.E.T.S ON LASER-ANNEALED POLYSILICON

Indexing terms: Field-effect transistors, Schottky-barrier devices

Schottky-barrier field-effect transistors (m.e.s.f.e.t.s) have been fabricated on uniformly doped laser-annealed polycrystalline silicon deposited on a silicon nitride insulator. The devices, which had aluminium Schottky-barrier gates and diffused n^+ sources and drains but nonoptimised channel profiles, had about 65% the g_m values of similar but optimised devices made on s.o.s. layers. Performance of these devices is considered adequate for certain innovative integrated-circuit technologies.

Introduction: Polycrystalline silicon, in which the crystallite structure has been altered by laser or electron beam annealing, has aroused considerable interest as a material offering potential for realisation of novel semiconductor device and circuit structures, such as multilevel integrated circuits. Tasch *et al.*[1] made laser-annealed polysilicon (l.a.p.) d.m.o.s.f.e.t.s, in which they measured an average mobility of 215 cm^2/Vs. Kamins *et al.*[2] made a 9-stage l.a.p. m.o.s. ring oscillator, measuring a mobility of 300 cm^2/Vs for their d.m.o.s.f.e.t.s. We report here the d.c. characteristics of a short-channel l.a.p. m.e.s.f.e.t., and compare them with those of a similar device made on s.o.s. D.M.E.S.F.E.T.s are relatively easy to make,[3] and may be faster than m.o.s.f.e.t.s with similar gate dimensions, but d.m.e.s.f.e.t. digital circuits are generally more complex than their enhancement/depletion-mode m.o.s.f.e.t. counterparts.

Processing: The starting material, prepared at Stanford University, was 500 nm of intrinsic l.p.c.v.d. polysilicon deposited on 100 nm of silicon nitride, which isolated the polysilicon from the underlying silicon substrate. A $1.5 \times 10^{12}/cm^2$ dose of phosphorus was implanted into the polysilicon at 100 kV. An 11 W argon ion laser with a 40 μm diameter beam was raster-scanned across the polysilicon, held at 350°C, at 12 cm/s; centre-centre spacing of the scans was 15 μm. The beam melted the polysilicon, uniformly distributing the dopant to a measured density of $3 \times 10^{19}/cm^3$. Surface profile measurements indicated that a surface ripple with an average peak-peak amplitude of about 80 nm remained after annealing.

The three-mask l.a.p. m.e.s.f.e.t. process, developed at Cornell University, began with the ion milling of source and drain windows in 180 nm of oxide. These n^+ regions were diffused from densified spun-on phosphorus-doped glass at 900°C for 20 min. L.A.P. mesas were then defined by wet etching, after which all the oxide was removed. The metallisation pattern was defined by lift-off of 250 nm of evaporated aluminium. The wafer was finally sintered in hydrogen at 500°C for 7 min.

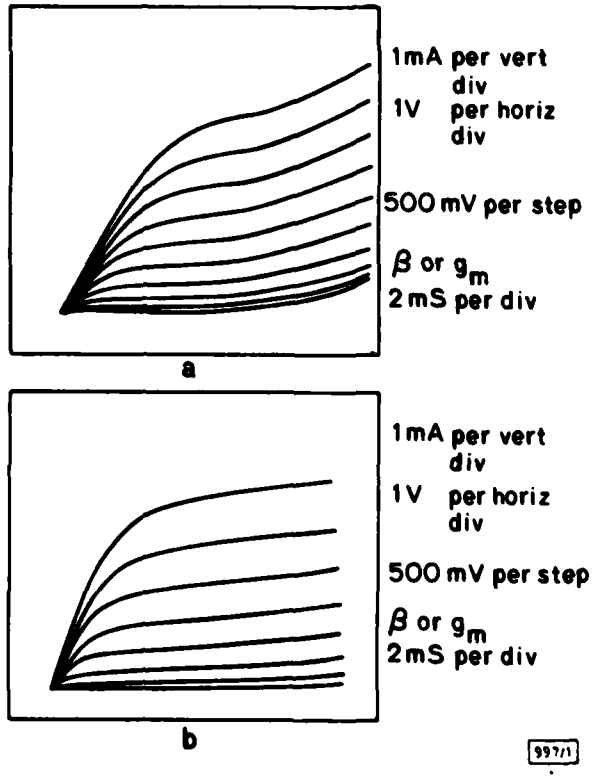

Fig. 1 *Drain characteristics of l.a.p. and s.o.s. m.e.s.f.e.t.s with aluminium Schottky-barrier gates 1 μm long × 200 μm wide, and source–drain spacing of 4 μm*

Results: The I/V characteristics of a 4 μm long × 50 μm wide test resistor exhibited conduction similar to that of two back-to-back diodes which had 'turn-on' voltages considerably less than 0·5 V. This phenomenon may be associated with the transport of electrons across the potential barriers at grain boundaries. The measured sheet resistance was 16 Ω/square; the lateral diffusion of 400 nm yielded an effective source-drain spacing of 3·2 μm. Using the resistor measurements, the average electron mobility in the layer was found to be 250 cm^2/Vs. For comparison, measurements of mobility made in 600 nm thick s.o.s. layers implanted with $1{\cdot}5 \times 10^{12}$/cm^2 of phosphorus at 150 kV resulted in a mobility value of 300 cm^2/Vs in the implanted region, which had its peak concentration about 400 nm above the Si/sapphire interface.[4] Hsu[5] has quoted similar results for s.o.s. layers. Average mobility values in the polysilicon layers are thus quite good.

Schottky-gate performance on these layers was also satisfactory. A test diode 3·2 μm long, 0·5 microns wide, and spaced from an n^+-diffused contact by 3·0 μm, exhibited 100 nA/μm^2 reverse leakage at −38 V bias. On m.e.s.f.e.t.s, the reverse-biased Schottky-gate leakage equalled this value at a drain bias of only −8·1 V, a result of the extremely high electric fields which exist at the drain edge of the gate in planar m.e.s.f.e.t. structures.[4] J/V measurements indicated that the barrier height was about 0·6 V for the Al Schottky diodes on l.a.p., virtually the same as has been measured for s.o.s.[3]

The performance of l.a.p. m.e.s.f.e.t.s was comparable to that of similar devices made on s.o.s. Drain characteristics of both types of devices are shown in Fig. 1. The l.a.p. m.e.s.f.e.t. had an offset-T centre-fed gate with a length of 1 μm and a width of 200 μm. The source–drain diffusion mask spacing was nominally 4 μm. After processing, it was found that 80 nm of the original 500 nm l.a.p. had been oxidised, resulting in a phosphorus pile-up at the surface, which could be deduced from the drain characteristics of the transistor at low drain voltages. The pile-up increases the g_m slightly compared with that of a device made on a uniformly doped layer of l.a.p. The saturated transconductance at $V_g = 0$ and $V_d = 5$ V was 125 ms per centimetre of gate width. The drain conductance g_d at $V_g = 0$ and $V_d = 7$ V was 200 mS, while the pinchoff voltage was −4·8 V. The s.o.s. m.e.s.f.e.t. of similar layout, but with a shallower ion-implanted channel, had a g_m of 200 mS/cm of gate width, a drain conductance of 140 μS and a pinchoff voltage of −3·8 V.

There is a noticeable kink in the drain characteristics of the l.a.p. m.e.s.f.e.t. at a drain voltage of about 7 V. Kamins *et al.*[2] observed a similar kink at drain voltages of about 5·5 V for m.o.s.f.e.t.s on l.a.p. with a source-drain spacing of 4 μm. This kink may be caused by a back-gating effect, in which electrons are accumulated at the bottom of the channel underneath the gate electrode, or by electron injection from the Si substrate through the thin nitride insulator. Two-dimensional simulations of these devices using CUPID[4] show that a field of several tens of thousands of kV/cm can exist in a direction normal to the interface, under the drain edge of the gate.

Discussion: The measured mobility of 250 cm^2/Vs is comparable to that measured by other workers for depletion-mode l.a.p. m.o.s.f.e.t.s and 83% of that measured on implanted 600 nm s.o.s. films. The potential barriers introduced by the grain boundaries cause the drain curves for conduction at low voltages to exhibit diode-like behaviour, which might make l.a.p. m.e.s.f.e.t.s unsuitable for use in very-low-voltage integrated circuits. Despite the grain boundaries, the Schottky barrier gates had low leakage and a reasonable breakdown voltage, comparable with that of gates made on s.o.s.

The saturated transconductance g_m of the l.a.p. m.e.s.f.e.t. can be increased by optimising the channel doping profile, either by ion implantation or by channel thinning. The pinchoff voltage of the l.a.p. device would also be reduced by these measures. More serious problems in these particular devices include the relatively large knee voltage of the l.a.p. m.e.s.f.e.t., and the kink in the drain characteristics, which might be a function of the nature of the insulating layer under the l.a.p.

Conclusions: The d.c. characteristics of an unoptimised l.a.p. m.e.s.f.e.t. are good, compared with those of s.o.s. m.e.s.f.e.t.s. Despite the influence of the grain boundaries on carrier transport at low electric fields, the l.a.p. m.e.s.f.e.t. has potential for use in both analogue and digital circuits and in novel structures, e.g. multilevel integrated circuits.

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14th March 1980

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One-Gate-Wide CMOS Inverter on Laser-Recrystallized Polysilicon

J.F. GIBBONS, FELLOW, IEEE, AND K.F. LEE

Abstract—A CMOS inverter having a single gate for both n and p channel devices has been fabricated using bulk silicon for the p channel device and a laser-recrystallized silicon film for the n channel device. The fabrication details and dc electrical performance of this device are described.

INTRODUCTION

Several recent publications have shown that 0.5 μm thick CVD Si films can be recrystallized by a scanning cw argon laser beam to produce material in which MOS devices can be fabricated directly [1]-[4]. In particular, Lee et al. [1] showed that both enhancement and depletion mode devices could be made on the *top* surface of such films using conventional techniques for fabrication of source and drain wells, gate oxidation, and so on. The channel mobilities deduced from the drain characteristics of these devices gave values that were found to be 60-70% of the values obtained on single crystal substrates. Q_{ss} values at the oxide/recrystallized polysilicon interface were found to be $10^{11}/cm^2$, which is device-worthy even though it is somewhat more than an order of magnitude higher than Q_{ss} for a high-quality oxide/single crystal silicon interface.

In a more recent paper, Kamins et al. [5] measured the interface properties that are obtained when a single crystal/SiO_2/polysilicon sandwich is exposed to laser radiation under conditions that recrystallize the polysilicon layer. They found that under appropriate processing conditions, Q_{ss} values at both the crystalline silicon/SiO_2 interface and the SiO_2/laser recrystallized polysilicon interface could be kept at or below the mid-$10^{10}/cm^2$ level. These results together with the previous results of Lee et al. led us to attempt to make a one-gate-wide CMOS inverter in which the bulk silicon is used for the p-channel device and the *bottom* of the laser recrystallized polysilicon film is used for its n-channel complement.

The basic device structure is shown in Fig. 1. The joint use of a single gate to drive both the n- and p-channel devices led Kleitman [6] to suggest the term JMOS to describe this structure. In what follows we discuss the fabrication and basic electrical characteristics of JMOS structures that were made to explore the central idea. The electrical characteristics obtained appear to warrant further investigation of the JMOS structure as a high packing density form of CMOS.

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EXPERIMENTAL

To obtain the highest surface mobility for the particle with the lower bulk mobility, it is preferable to build the p-channel device in the single crystal substrate. Accordingly, fabrication is performed on an n-type <100> single crystal of Si of resistivity 1-4 Ω-cm. A layer of 5000 Å of field oxide was thermally grown on this material, after which source and drain regions were defined by photolithographic patterning and chemical etching. A boron predeposition was then done at 950°C for 30 min., followed by a 900°C, 15 min. dry O_2 oxidation. The field oxide was removed at the gate region by another patterning step, and 1000 Å gate oxide was grown at 1000°C in dry O_2. A layer of 1 μm of CVD polysilicon was then deposited as the gate material, followed by a $POCl_3$ predeposition at 975°C for 30 min. to dope the gate. 2000 Å of CVD SiO_2 was then deposited and the gate was defined by a photolithographic patterning step plus chemical etching of the CVD SiO_2 and polysilicon. The gate dimensions utilized in these experiments were 100μ/50μ (W/L). After fabrication of the gate, the CVD SiO_2 was removed by chemical etching, and 1000 Å SiO_2 was grown on the gate polysilicon at 1100°C in dry O_2. A layer of 0.5 μm of CVD polysilicon was then deposited, followed by a B^+ implant of $1 \times 10^{12}/cm^2$ at 100 keV. This layer of CVD polysilicon acted as device material for the n-channel device on the top level. A thermal anneal at 1100°C in N_2 for 1 hour was carried out to improve the surface structure during subsequent laser recrystallization [3]. A scanning cw argon laser was used, with a laser power of 10W, a spot size of 40μm, a scan speed of 12 cm/sec, a step size of 15μm, and a substrate temperature of 350°C. The top level device region was defined by deposition of 2000 Å of CVD SiO_2, a patterning step, and chemical etching of the CVD SiO_2 and laser recrystallized polysilicon. The CVD SiO_2 was then removed. 5000 Å of CVD SiO_2 was deposited to cover up the structure and densified at 900°C. Source and drain regions to the top level devices were defined and formed by a $POCl_3$ predeposition at 975°C for 30 min. Contact holes were then defined. Al was evaporated, patterned and alloyed at 450°C in N_2 for 30 min. to complete the structure.

DEVICE CHARACTERISTICS

The drain characteristics of devices obtained from the

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fabrication schedule outlined above are shown in Fig. 2(a) and 2(b). In part (a) we show the drain characteristics for the p-channel device, which was made on the single crystal silicon. From analysis of these drain characteristics we find a threshold voltage of -2.2 volts and a surface mobility for holes of 180 cm^2/V-sec. These values are consistent with a Q_{ss} value of approximately 1.6×10^{11}; threshold shifting could be performed using conventional implantation techniques and thermal annealing prior to fabrication of the gate as outlined above.

The drain characteristics for the n-channel device are shown in Fig. 2(b), and lead to a threshold voltage of 2.1 volts and a surface mobility for electrons in the laser recrystallized film of 160 cm^2/V-sec. These values are somewhat lower than those obtained in previous experiments [4] but nonetheless sufficient to indicate that well-machined CMOS devices can be made in the two-level ("high-rise") configuration envisaged as JMOS.

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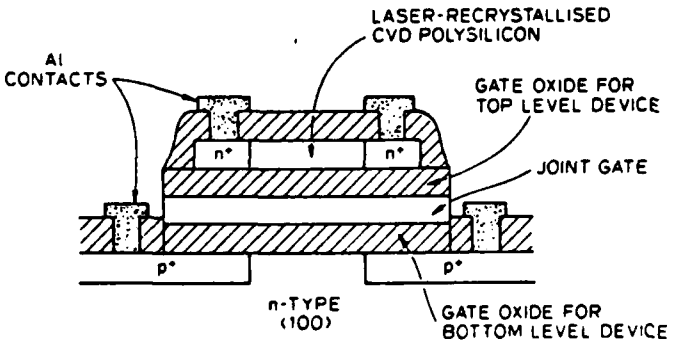
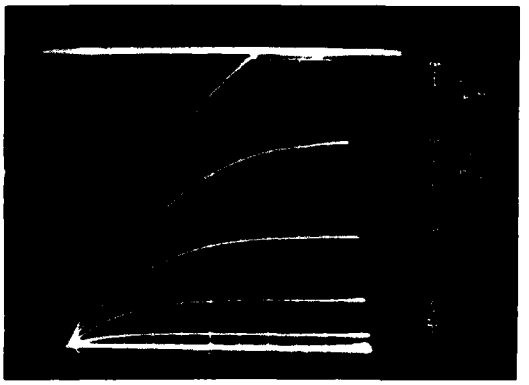


Fig. 1. Schematic of a JMOS structure.



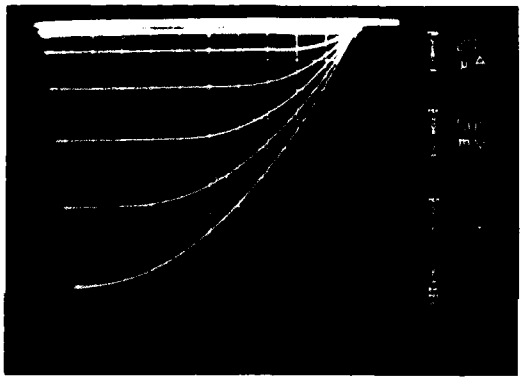


Fig. 2. (a) I-V characteristics of upper-level n-channel enhancement mode device fabricated in laser-recrystallized polysilicon, V_G = 7 V to 0 V.
(b) I-V characteristics of lower level p-channel enhancement mode device fabricated in single crystal, V_G = -7 V to 0 V.

cw laser recrystallization of ⟨100⟩ Si on amorphous substrates

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A polycrystalline silicon film 0.55 μm thick was deposited in a low-pressure CVD reactor on a Si_3N_4 substrate. Islands of various sizes (2×20 μm up to 20×160 μm) were prepared by standard photolithographic techniques. Laser annealing was then performed under conditions which are known to cause an increase in grain size from ~500 Å to long narrow crystals of 2×25 μm in a continuous polysilicon film. These same conditions were found to produce single-crystal ⟨100⟩ material in the (2×20 μm) islands. However, 25×25-μm and 20×160-μm islands remain polycrystalline after the laser scan.

PACS numbers: 72.80.Ng, 81.15.Gh, 81.40.Ef

Recent literature describes the use of both pulsed and cw laser and electron beams to anneal ion-implantation damage in semiconductors[1-5] and to recrystallize amorphous films.[6-8] Most studies of the cw laser system have been concerned with the annealing of shallow implantation-amorphized layers on top of single-crystal material, though Laff and Hutchins[9] and Gat *et al.*[10] also report on the use of a cw laser for recrystallization of CVD silicon films on amorphous substrates.

In the study of Gat *et al.*,[10] ~0.4-μm-thick *continuous* polycrystalline films having an initial average grain size of ~500 Å were prepared by low-pressure chemical vapor deposition on a Si_3N_4 substrate. The films were held at a temperature of 350 °C during laser annealing. The annealing was accomplished with an Ar^+ laser having an output of 11 W focused into a 40-μm spot and scanned across the film at a rate of ~12 cm/sec. Under these conditions, major structural changes in the polycrystalline film were found to occur. Using TEM, columnar crystallites were found to extend completely through the film to the nitride interface. The crystallites had a typical surface geometry of $\sim2\times10$ μm and were found to develop at an angle to the direction of the scan, producing a chevronlike structure. In the center of a laser-scan line the crystallites were aligned parallel to the scan direction and had a maximum length of ~32 μm and an average width of ~2 μm. The crystallites displayed a number of crystal orientations with no indication of a perferred orientation. Subsequent work by Lee *et al.*[11] has shown that melting must occur throughout the film for the long crystallites to form.

The objective of the present study was to determine whether single-orientation single-crystal material could be formed by patterning the polycrystalline film prior to annealing. This possibility is suggested by the work of Smith *et al.*,[12] who found that single-crystal KCl could be grown by depositing the KCl on very finely engraved quartz substrates. It should be emphasized, however, that in the present experiments the substrates were *not* engraved or specially prepared in any way. Rather, the polycrystalline film was simply etched to define islands of various sizes.

The polysilicon samples used for this study were essentially identical to those used by Gat *et al.*,[10] Polysilicon layers approximately 0.55 μm thick were deposited in a commercial Tempress reactor. The substrates were crystalline Si onto which had been deposited a 1000-Å layer of Si_3N_4 (LPCVD). Islands of polycrystalline Si were then formed by standard photolithographic techniques. The islands ranged in size from 2×20 μm to 20×160 μm. The 2×20-μm islands were arranged with the long dimension both parallel and perpendicular to the laser scan direction.

After formation of the islands, some of the wafers were multiply implanted with phosphorus according to the following schedule: 3×10^{14}/cm^2 at 50 keV, 6×10^{14}/cm^2 at 100 keV, 10^{15}/cm^2 at 150 keV, and 6×10^{15}/cm^2 at 100 keV.

The samples were then irradiated in the scanning apparatus described in Ref. 6. A cw Ar^+ laser (Spectra Physics

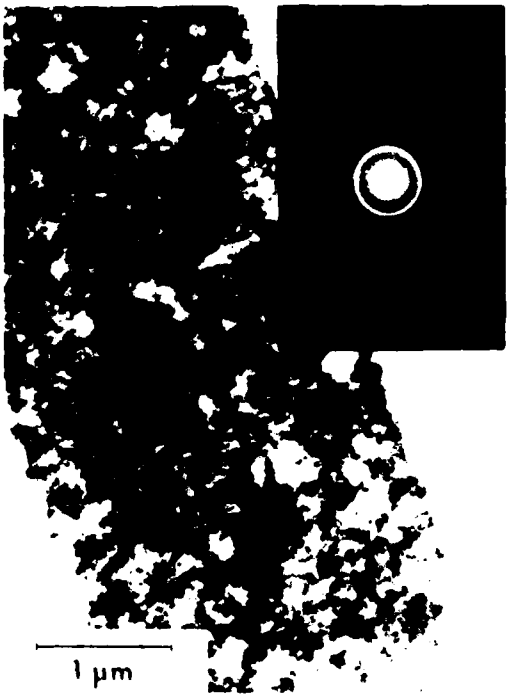

FIG. 1. Electron micrograph of as-deposited (unannealed) island structure and selected area diffraction pattern (right inset) typical of region

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(a) (b)

FIG. 2. Electron micrographs of laser-annealed island arrays. (a) Scanning electron micrograph of laser-annealed islands on Si_3N_4 film; (b) bright-field transmission electron micrograph of laser-annealed island structure and selected area diffraction pattern (right inset) typical of region.

Model 171-09) was used in the multiline mode. The samples were held to a heated brass sample holder by a vacuum chuck during annealing. Sample temperatures of 350 °C were used for all experiments reported here. The laser was focused into a 40-μm spot. Two laser power/scan rate conditions were used: 9 W at ~0.15 cm/sec and 11 W at ~12 cm/sec.

Nomarsky optical observation of the annealed films revealed smooth featureless surfaces in all 2×20-μm islands, independent of their orientation with respect to the scanning direction. Featureless surfaces were also observed on 12×30-μm L-shaped islands. However, the 20×160-μm islands show surface structure similar to that obtained by Gat *et al.*[10] on continuous films, independent of the orientation of the island with respect to the beam.

In Fig. 2(a) a representative scanning electron micrograph of a patterned poly-Si stripe ($2\times 20\,\mu$m) array after scanning laser annealing is shown. No significant alterations in the morphology or geometric features of the stripe patterns were observed in any of the individual island structures examined after laser annealing for either of the laser power/scan rate conditions employed. In addition, the surfaces of the stripes shown in Fig. 2(a) appear smooth and structureless with an apparent absence of surface roughness typically noted in as-deposited polycrystalline films.

To examine the internal microstructure and crystallinity of the island structures, we prepared samples for TEM/TED analysis using a jet thinning technique. In all cases a thin ($\simeq$300 Å) nitride layer remained suspended across a central hole with the poly-Si islands available for observation in the electron microscope. The as-deposited island structures were composed of polycrystalline grains ranging from 200 to 500 Å in average size. In all cases selected area diffraction patterns showed continuous ring patterns that are typically of (fine grained) polycrystalline films (see Fig. 1.). In contrast, the ion-implanted structures showed an absence of structure and the recorded diffraction plates exhibit the expected amorphous patterns.

After laser annealing, the 2×20-μm islands show an absence of fine-grained or amorphous structure and are completely recrystallized to form single-crystal stripes on the amorphous Si_3N_4 substrate [Fig. 2(b)]. Identical results were obtained in both the as-deposited (polycrystalline) and ion-implanted (amorphous) stripes, suggesting that the formation of recrystallized single-crystal islands is relatively independent of the initial crsytalline state of the starting material for the experimental conditions used in this study.

Throughout the entire length of the stripe shown in Fig. 2(b) there are no microscopic defects, and selected area diffraction patterns (right inset) indicate that the island is single crystal and of (100) orientation. In all of the island structures examined thus far we have detected *only* the (100) orientation. Of additional interest is the fact that the recrystallization is not dependent on the relative positioning of the island structure with respect to laser scan direction. Experiments conducted on samples in which the laser scan direction was parallel or perpendicular to the long axis of the strip exhibit identical results with no apparent differences in structure.

To further investigate the crystallinity of the island structures we then removed approximately one-half of the thickness of the island structures by chemical thinning, leaving the Si_3N_4 film intact as a support membrane. Selected area diffraction again showed only single-crystal (100) patterns, confirming that recrystallization occurred throughout the entire thickness of the island.

Examination of the larger ($20\times 160\,\mu$m) island structures and "L-shaped" arrays ($12\times 30\,\mu$m) showed that laser annealing resulted in the formation of large polycrystalline grains of 10-μm maximum length, typically arranged in a chevron pattern pointing in the direction of the laser scan. This is similar to results reported by Gat *et al.*[10] The occurrence of stacking faults was also noted in some structures, independent of island dimensions. The nucleation of stacking faults is not thought to be essential for regrowth since smaller single-crystal islands arrays and large columnar structures are observed containing no stacking faults or other microscopic defects.

From the data obtained we can conclude that defect-free single-crystal Si stripes of (100) orientation can be formed on amorphous Si_3N_4 films by laser annealing. It is apparent that the formation of these single-crystal arrays may be size restricted. Additional experiments are currently in progress to determine both the limiting parameters influencing single-crystal nucleation and the influence of pattern dimensions on the mechanisms of regrowth. Parameters being considered are the surface roughness of the nitride film and the stresses generated by the island/nitride interface, the influence of the polysilicon film thickness, and the effects of the power/scan rate condition.

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LPE Growth of Silicon from Poly Si/Si Structure Using CW Argon Laser

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ABSTRACT

Epitaxial layers were grown by melting the surface of a polysilicon/silicon structure with a scanning cw argon laser beam. Topographical features and crystalline perfection associated with the laser-induced recrystallization were investigated by transmission electron microscopy (TEM) and optical microscopy. The regrown layers obtained were relatively free of defects, as revealed by TEM analysis. Large concentrations of dislocation lines and twinning zones were not detected in these studies; however, dense dislocation networks were observed in the substrate beneath the epitaxial layer.

Laser annealing, particularly by cw laser scanning, has been used in a variety of experiments to grow thin layers of silicon crystal. Recrystallization of an ion-implanted amorphized layer (1-4), grain growth of both poly and single crystal silicon on an insulating layer (5, 6), and graphoepitaxy (7, 8) are the major achievements obtained to date.

However, epitaxial growth from the polysilicon/single crystal silicon structure, utilizing cw laser scan techniques has not been reported, although epitaxial growth (9-12) and bridging epitaxial growth (13) are known to occur by melting the surface with a high energy density ($10^7 \sim 10^8$ W/cm^2) laser pulse.

This paper describes the grain growth obtained when a poly-Si/Si structure is scanned by a separated single beam of a cw Ar laser, with an energy density high enough to melt the surface. Under appropriate conditions, epitaxial growth of silicon is obtained.

* Electrochemical Society Active Member.
Key words: semiconductor, epitaxy.

Experimental

The scanning laser setup has been described elsewhere (14). It consists of a 25W cw Ar laser operated in a multiline mode, an X-, Y-beam deflection system implemented with galvanomirrors, a heated vacuum-chuck sample holder, and control electronics.

The samples were prepared by depositing 2000Å polysilicon layers on (100) Si wafers using the hydrogen reduction of silane at 630°C at 0.8 Torr (LPCVD). The grain size was on the order of 500Å or less as measured by transmission electron microscopy (TEM).

The scanning speed of the laser beam was 12 cm/sec. In area scan experiments, the separation between the two successive scanning lines was set to about 11 μm so that the melted zones were well overlapped to assure the occurrence of uniform growth over the total area scanned. This assures overlap of more than 50%

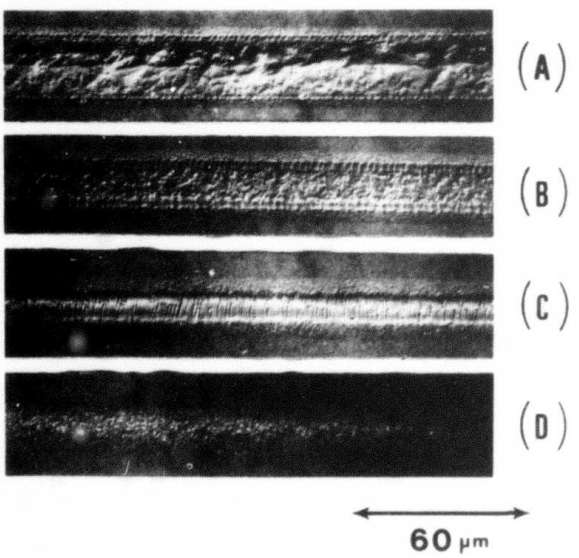

Fig. 1. Optical micrographs showing the surface topography induced after single line scans: (A) 10W, (B) 9W, (C) 8W, (D) 7W.

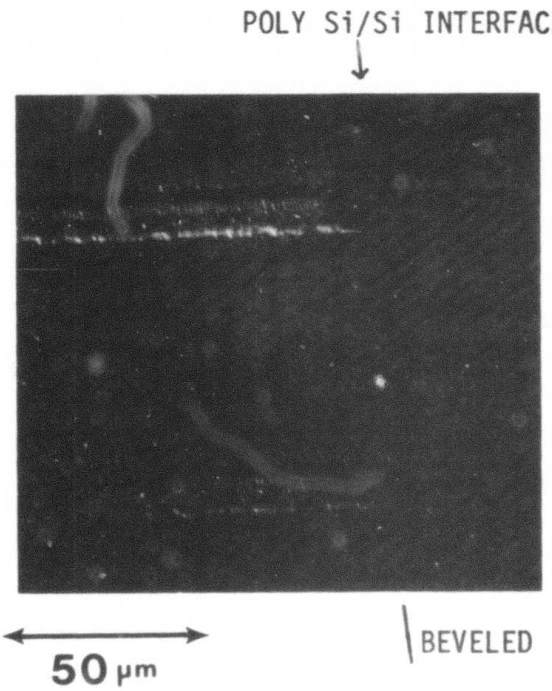

Fig. 2. Laser traces on a beveled and etched sample

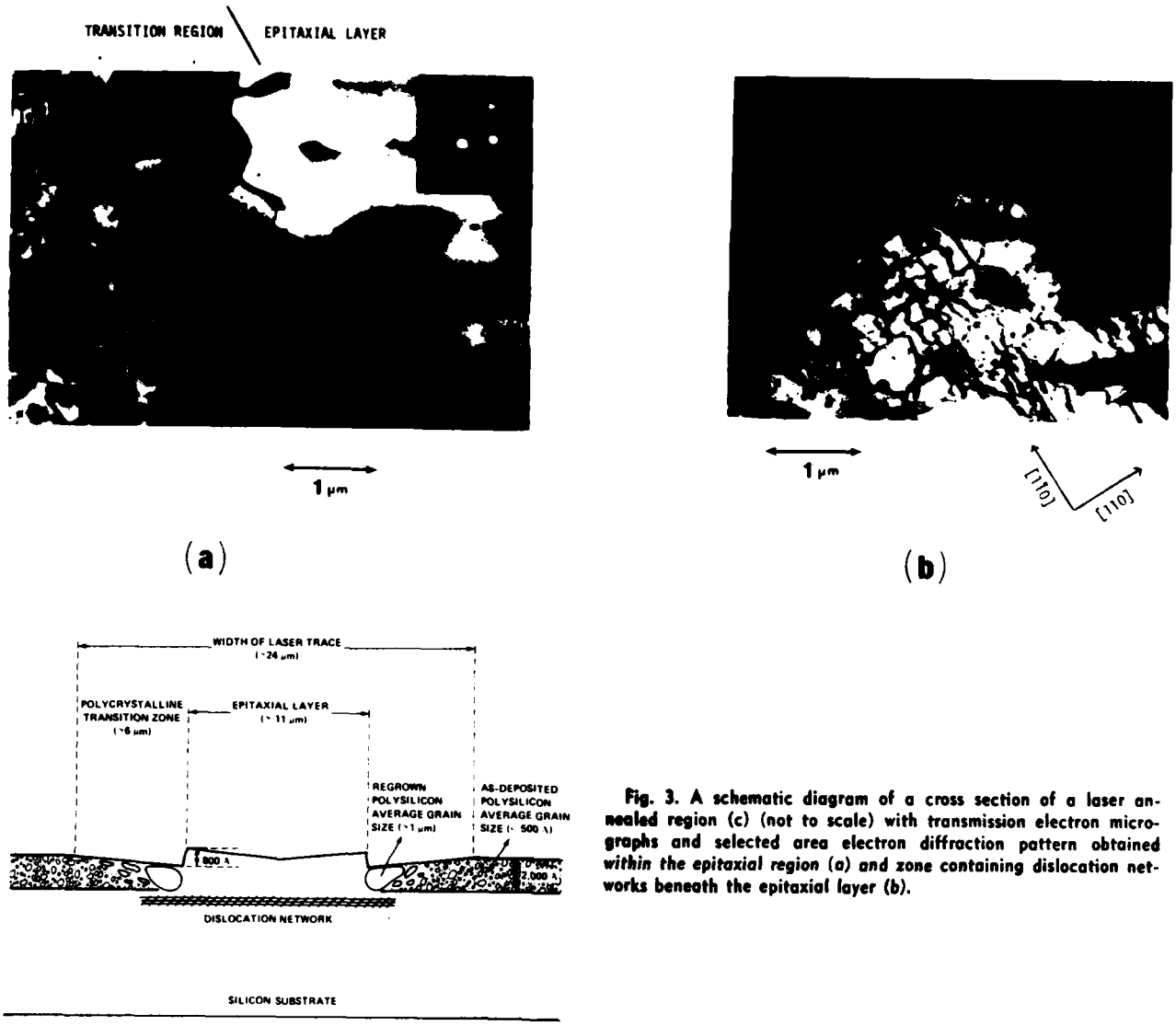

Fig. 3. A schematic diagram of a cross section of a laser annealed region (c) (not to scale) with transmission electron micrographs and selected area electron diffraction pattern obtained *within the epitaxial region (a) and zone containing dislocation networks beneath the epitaxial layer (b).*

of the laser traces. The substrate temperature was 350°C in all anneal experiments. Bevel polishing was done at an angle of 1°9′ on a Plexiglas plate with Metadi grits. The etchant used to delineate the polysilicon/silicon substrate boundary was a diluted Sirtl etch with the composition CrO_3:H_2O:HF = 5g:10 ml:1 ml.

Results

The samples were annealed under various output powers in the single line scan mode. The development of surface topographic features with the output power of the cw laser is shown in Fig. 1. At low power, the trace of a laser beam shows a dotted surface structure [Fig. 1D)], which was found to be a result of the grain growth of polycrystalline silicon when examined by TEM. Increasing the laser power to a threshold value turned the center portion of the beam trace band into a ripple pattern [Fig. 1(C)]. Further increase in laser power smeared out the ripples into a rather coarse and irregular pattern [Fig. 1(A) and (B)]. Although the dotted and ripple structures have already been reported in pulse experiments (12), the latter irregular feature was not known. It did not disappear even at an output power level as high as 15W which is the maximum output of the cw laser used in this experiment. This can be associated with the longer melt duration in the cw laser irradiation than that in the short pulse case.

The bevel polish and etching show the existence of the polysilicon/single silicon substrate boundary in samples annealed at low laser powers. However, the boundary disappeared under the ripple pattern indicating that melting occurred into the substrate and suggesting the epitaxial regrowth of the polysilicon layer (Fig. 2). The beveling also shows the minute variation of the cross-sectional height of the beam trace as illustrated in Fig. 3(c). TEM examination of these single line scanned samples was employed to study the possible occurrence of epitaxial growth.

The change in the crystal structure brought about by cw laser anneal is shown in Fig. 3(a) for an 8W annealed sample with the ripple structure. The grain size of polycrystals increases from the edge toward the center of the laser beam trace and turns into single crystal epitaxial layer at the onset front of the ripple structure. The quality of the epitaxial layer is good as judged by the (100) transmission electron diffraction pattern, and by the absence of twin boundaries or dislocation lines. However, the electron micrograph of the epitaxial layer shows a periodic contrast associated with surface undulations, thereby duplicating the characteristic ripples observed on the surface of the regrown layer. This periodic ripple (thickness) contrast can probably be ascribed to the periodic change of stress accompanying crystal regrowth. The regularly defined (thickness) contrast variations disap-

peared in the sample annealed at 10W. The layer grown at 10W was also shown to be single crystal by diffraction, with no structural irregularity observed by TEM.

Another feature revealed by the TEM observation is the dislocation network which appeared in the substrate crystal below the epitaxial layer [Fig. 3(b)]. From micrographs obtained on a large number of samples, we observed that the dislocation lines extend from the epitaxial layer to the transition region where polycrystals develop, depending on the laser energy they receive. Since no periodic variation in contrast is observed for long dislocation lines, with the foil oriented at the exact Bragg condition ($S_g \simeq 0$), these lines are believed to lie on (100) planes extending in <110> directions. All these results are summarized in Fig. 3(c), which schematically shows the crystallographic changes when a surface of a polysilicon/silicon structure is swept by a laser beam.

Area scanning was used in an attempt to obtain large epitaxial layers. Scan conditions were chosen as stated in the Experimental section, using the results obtained for single line scan experiments. The surfaces of the area scanned sample are seen to reflect the topographical features of single line scans. One example is shown in Fig. 4, which retains the ripple structure observed in a single line sample. Electron diffraction demonstrates that the polysilicon layer was regrown as an epitaxial layer by area laser beam scanning.

Discussion

A lower bound on the propagation velocity of the recrystallization front along the direction of scan can be estimated, postulating that the ripples are generated by standing waves from interference of laser beam on crystal surface (12, 16, 17).

This propagation velocity should be an order of magnitude faster than the scan speed, because the crystal growth pattern (the ripples) caused by the variation of laser power distribution by interference is not smeared out by scanning. Therefore, the lower limit of this velocity is estimated to be around 1 m/sec in the ripple growth condition. This value is well within a reasonable range for the laser-induced liquid phase epitaxial growth, from the discussion on the crystal growth velocity in a previously published paper (15).

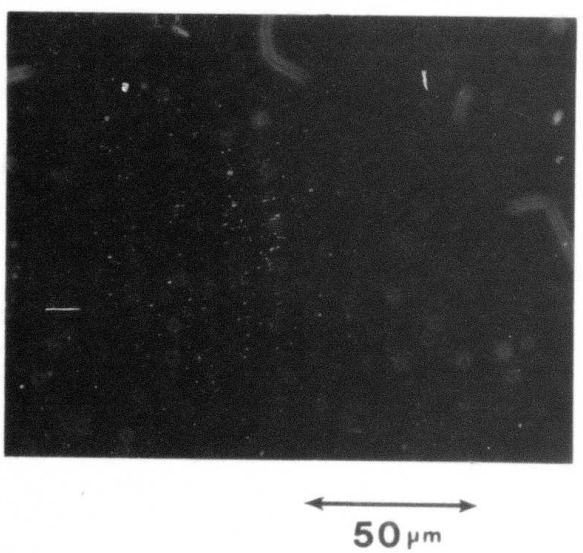

Fig. 4. An optical micrograph showing the surface topography of an epitaxial layer grown by overlapping laser scans (8W).

Conclusion

Liquid phase epitaxial growth from polysilicon/single crystal structures utilizing a cw Ar laser was demonstrated. The epitaxial layer was of relatively good crystal perfection in that the layer included few dislocations and twins. However periodic pile up of stress at some power levels, surface roughness, and high density dislocations under the epitaxial layer indicate the need for further study.

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Lateral Epitaxial Recrystallization of Deposited Silicon Films on Silicon Dioxide

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ABSTRACT

A scanning cw argon laser has been used to epitaxially recrystallize silicon films deposited over exposed regions of single crystal silicon substrates and cause the lateral extension of these epitaxial regions into the portions of the silicon film deposited over oxide-covered regions of the substrate. Planar and cross-sectional transmission electron microscopy were used to investigate the microstructure, which is consistent with melting and liquid-phase regrowth.

In a recent report, Tamura *et al.* (1) have demonstrated the possibility of "bridging epitaxy" in which a single crystal silicon substrate is used as a seed for the laser recrystallization of a silicon film over silicon dioxide. The regrowth of the deposited film starts where the film contacts the substrate and extends laterally into the portion of the silicon film on top of the insulating oxide layer. Such a single crystal film would find many applications in integrated circuit technology.

In their experiments, Tamura *et al.* used a Q-switched ruby laser to melt the silicon layer deposited on the single crystal silicon wafer which was partially covered with oxide stripes. Using planar transmission electron microscopy, they observed the vertical epitaxial growth of the deposited silicon as it solidified over the exposed silicon substrate and some lateral extension of the single crystal material over the oxide-coated areas.

A pulsed laser, however, melts a large region of material which then solidifies in a manner primarily determined by heat transfer away from the molten areas. In this manner, Tamura *et al.* proposed that the regions over the exposed single crystal substrate crystallized before the silicon over the oxide because the low thermal conductivity of the oxide layer kept the film in these regions above the melting point for a longer time.

The use of a scanning cw laser would appear to be an attractive alternative to the pulsed laser for this application. The epitaxial regrowth process could start over the exposed silicon substrate, and then the molten zone could be moved into the film over the oxide-covered regions in a more controlled manner.

In this report we describe the use of a cw argon laser to epitaxially recrystallize silicon films over exposed regions of a single crystal silicon substrate and the lateral extension of these epitaxial regions into the deposited silicon film over oxide-covered regions of the substrate. Planar and cross-sectional transmission electron microscopy were used to reveal the structure both in the plane of the film and perpendicular to it.

Sample Preparation

Silicon wafers with (100) orientation were oxidized at 1000°C in a TCE/O_2 atmosphere to form a 1000Å thick oxide layer. The oxide was then patterned using a mask containing rectangles of varying sizes from 50 × 50 μm to 150 × 300 μm, and the oxide was removed from the orthogonal, 12 μm-wide grid lines separating the oxide rectangles. Silicon films were then deposited in a low pressure, chemical vapor deposition reactor onto both exposed substrate and the oxide-covered regions. (The wafers were cleaned with dilute HF no longer than 5 min before insertion into the LPCVD reactor.) Two different deposition temperatures were used: 550° and 625°C. Films deposited at 625°C have been shown to have a columnar, polycrystalline structure, while those deposited at 550°C are initially amorphous (2). Both types of film were deposited to a thickness of approximately 2000Å. For comparison with the regrown structure to be discussed below, Fig. 1 shows a cross-sectional TEM of an unrecrystallized area of 625°C polysilicon from one of the same wafers as the laser-recrystallized samples. The expected columnar, (110)-oriented grains are apparent (2, 3).

In an attempt to make the deposited layer and the surface region of the underlying single crystal substrate amorphous and facilitate regrowth, some of the structures were then implanted with a dose of 3×10^{15} cm^{-2} silicon ions while the substrate was held on a liquid-nitrogen-cooled support. The implant energy of 135 keV placed the peak of the implant close to the substrate-film interface.

After implantation, the deposited films were recrystallized with a cw argon laser at Stanford (4). The laser beam was moved by galvanometer-controlled mirrors. A 135 mm focal length lens was used, and the spot size on the wafer surface was 40 μm. The retrace was blanked so that the trace of the laser beam on the wafer surface was always in one direction. The scan speed was 12 cm/sec, and a power of 9.5W was used. With the given scan speed and spot size, this power appears to be optimum. At significantly lower powers, the

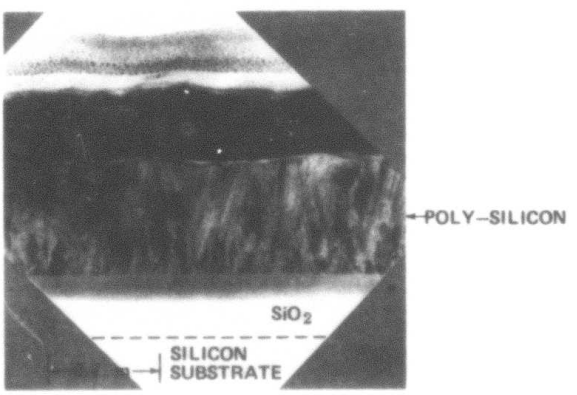

Fig. 1. Cross-sectional TEM of unrecrystallized polysilicon film deposited on silicon dioxide.

* Electrochemical Society Active Member.
Key words: laser recrystallization, silicon film, epitaxial growth.

large-grained regions do not overlap, especially over the single crystal silicon with its high thermal conductivity. At much higher laser powers, the silicon over the oxide tends to agglomerate, and the substrate may be damaged. Other satisfactory combinations of laser parameters are, of course, possible.

After completion of the recrystallization, the wafers were returned to Hewlett-Packard for analysis. Suitable control wafers were thermally annealed for comparison with laser-recrystallized samples. These wafers were inserted into a standard diffusion furnace at 550°C and annealed for 5 hr before the temperature was ramped to 650°C for 2 hr and then to 950°C for 1 hr.

After preliminary observation with optical and scanning electron microscopes, planar and cross-sectional samples were prepared (5) from the various wafers and examined in a Siemens Model 101 transmission electron microscope. Some samples were also chemically etched using Secco etch to reveal grain boundaries.

Results and Discussion

Optical microscopy and SEM analysis of the regrown material showed regions of varying thickness over the oxide-covered areas of the substrate (deduced from interference colors) and also surface ripples, especially over the exposed substrate, probably due to optical interference effects, as has been described previously (6). The silicon film extending into the oxide-covered regions in the direction of the laser scan appeared to be especially smooth. Etching to delineate grain boundaries revealed fewer boundaries near the oxide step than farther onto the oxide-coated rectangles. These preliminary observations support the more detailed TEM analysis, although they cannot be considered definitive. A scanning electron micrograph of an unetched sample is shown in Fig. 2 to place the transmission electron micrographs to be discussed next in context. The laser scanned the sample from left to right. Thickness nonuniformities perpendicular to the scan direction are seen at the trailing edge (left side of oxide cut).

Cross-sectional TEM's of one sample are shown in Fig. 3. This sample contained a deposited layer of initially polycrystalline silicon and was implanted with silicon to disrupt any barrier to recrystallization at the film-substrate interface. The scan direction was again from left to right. Figure 3c shows the deposited film directly over the exposed single crystal substrate, and the other portions of the figure show the silicon film extending over the oxide steps. (The speckled region above the deposited film is the epoxy used in preparing the cross-sectional TEM's). Figure 3 and detailed comparison of the relevant electron diffraction patterns confirm that the film directly over the single crystal substrate has recrystallized epitaxially; the crystal orientation is the same in the film as in the substrate, and the film contains few defects. The planar TEM of Fig. 3d reveals that the defects at the substrate-film interface seen in Fig. 3d are an orthogonal array of misfit dislocations propagating from the oxide step. These misfit dislocations were not observed in all regions, suggesting that they can be avoided by proper processing conditions. Occasionally, twins and inclined dislocations were seen extending from the substrate-film interface, as schematically indicated in Fig. 3f.

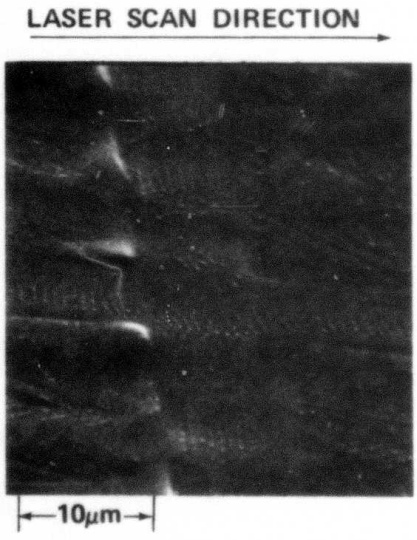

Fig. 2. Scanning electron micrograph of laser-recrystallized silicon film deposited over exposed silicon lines and oxide-covered rectangles. The laser beam scanned the sample from left to right.

Figure 3e shows the silicon film extending onto the oxide layer. Detailed examination in the TEM reveals that the crystal orientation of the film is the same as that of the substrate, although variation of the thickness of the cross section makes comparison of the orientations directly from the photomicrographs difficult. Although some defects are seen in the film, no grain boundaries are visible within the portion of the film seen in the micrograph. Since this is the leading edge of the laser scan, where the laser moves from the part of the film over the substrate onto that over the oxide, the scanning beam is expected to extend the single crystal region of the film significantly in the lateral direction. Optical microscopy after grain boundary etching does, indeed, suggest that the single crystal region extends farther on this side of the oxide cut than on the other side, although the asymmetry is not clearly revealed by the cross-sectional TEM's, which sample only one isolated area. This observation suggests that two different mechanisms may dominate on the two sides of the oxide cut.

These cross-sectional TEM's reveal several other important features. Most obvious is the mass transport caused by the laser recrystallization. Since the deposited film initially has a uniform thickness of approximately 2000Å, a 1000Å-high step should appear at the top of the deposited film, replicating the oxide step. This step is not seen in Fig. 3e. On the thermally annealed samples, which remained solid during the recrystallization, the expected step of 1000Å was observed.

The opposite side of the oxide cut is seen in Fig. 3a and b. As on the right side, the crystal extends continuously over the oxide step. In this case the grain is seen to terminate at the left approximately 0.5 μm from the edge of the oxide step. Because the laser beam approaches this region from the area which contains a buried oxide layer, rather than from the region with the exposed substrate, the recrystallization mechanism may be quite different than on the opposite side. On the trailing edge there should be no marked tendency of the laser beam to "drag" a single crystal region away from the oxide edge. The controlling mechanism on this side could be similar to that described in experiments with the pulsed laser (1) where the low thermal conductivity of the oxide causes the silicon above it to remain molten longer than that over the exposed substrate. If the major heat loss is by lateral heat transfer toward the oxide cut, the solid silicon would propagate from the oxide edge, and lateral single crystal growth is possible. Although a step is seen at the top of the silicon film where it crosses the edge of the oxide, the step is much less abrupt and of less height than the oxide step. For comparison, the shape seen on the thermally annealed sample is shown by the dashed line superimposed on Fig. 3a. The silicon film on top of the oxide is also seen to be much thinner than that directly over the substrate, indicating significant mass transport, as is shown by the SEM of Fig. 2.

Near both edges of the oxide cut, defects are seen in the substrate. One might speculate that these defects

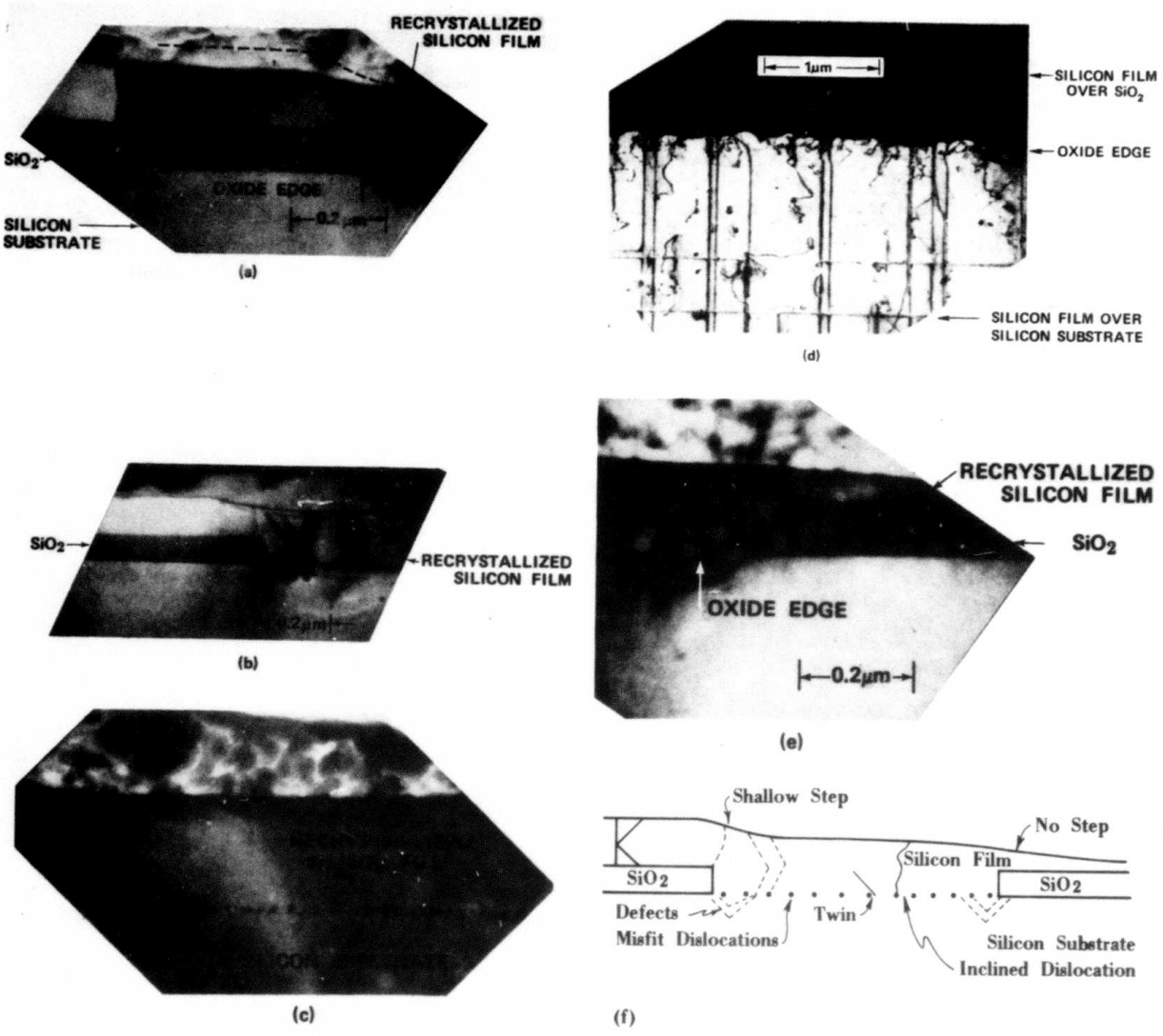

Fig. 3. Cross-sectional and planar TEM's of laser recrystallized silicon film: (a) and (b) over oxide steps at left of oxide cut (b is a dark-field micrograph); (c) over exposed single-crystal substrate; (d) planar section, primarily over exposed substrate; (e) over oxide step at right. (f) Schematic representation of features observed. The scan direction was from left to right in all except (d).

arise from relaxation of stress discontinuities caused by the different thermal expansion coefficients of silicon and silicon dioxide (3×10^{-6} compared to 0.5×10^{-6}/°C), as well as by temperature differences over silicon- and oxide-covered regions. Not only are defects observed extending into the substrate, but slip dislocations parallel to the wafer surface have also been seen several microns beneath the surface of the substrate. These have been observed both under the oxide and under the oxide cuts. These deep-lying dislocations are probably caused by thermal stresses associated with scanned beam recrystallization.

The regrowth of the initially amorphous films was similar to that of polycrystalline films in the regions which were melted. Surrounding the melted regions, of course, were regions where the initially amorphous film was converted to polycrystalline silicon, probably by solid-phase crystallization.

Observation of laser-recrystallized samples with and without the silicon implant showed little difference, with epitaxial regrowth over the single crystal substrate and defects at the interface. This suggests that the implantation is not needed in the case of liquid-phase recrystallization. The lack of epitaxial regrowth in the case of the thermally annealed sample indicates that the implant dose was insufficient to disrupt the interfacial layer present because of the deposition conditions and to allow solid-phase regrowth, even though the dose was sufficient to amorphize the surface regions of the silicon substrate beneath the interface. We speculate that a dose of 10^{16} cm^{-2} might produce the necessary disruption of the interfacial layer to allow solid-phase regrowth.

The different behavior on the two sides of the oxide cut leads us to suggest the following modification of the experimental structure. If the polysilicon is etched from part of the oxide cut and the laser scanning direction is such that laser-assisted growth is started where the polysilicon contacts only the underlying single crystal and proceeds over a gradually beveled oxide step, superior results might be achieved, including the possibility of solid-phase regrowth.

Conclusion

A scanning cw argon laser has been used to epitaxially regrow deposited silicon films over exposed regions of a single crystal silicon substrate and cause the lateral extension of these epitaxial regions into the deposited silicon film over oxide-covered regions of the substrate.

This process occurred by melting and liquid-phase regrowth.

Acknowledgment

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PROPERTIES OF MOSFETS FABRICATED IN LASER-ANNEALED POLYSILICON FILMS

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Enhancement-mode and depletion-mode MOSFETs of 3 μm gate lengths have been fabricated with the transistor channels in thin films of polycrystalline silicon annealed with a scanning cw argon laser. Device performance of the transistors was comparable to those fabricated in single crystal silicon. A nine-stage ring oscillator was also fabricated. Minority carrier generation lifetime of the order of 10^{-9} sec. was measured in the laser-annealed polysilicon.

1. INTRODUCTION

Previous experiments with a scanned cw argon laser on polysilicon as prepared by low pressure chemical vapor deposition (LPCVD) has produced a significant increase of grain size, from 500 A to 2μ x 25μ, and a reduction of resistivity by about a factor of two (1).

Enhancement-mode and depletion-mode MOSFETs have been fabricated with the channels in the laser-annealed polysilicon (2). Device performance of the laser-annealed polysilicon was comparable to single crystal silicon and far superior to conventionally prepared polysilicon. To test the feasibility of fabricating such devices of smaller dimensions, subsequent fabrication was done at Hewlett-Packard and Texas Instruments.

II. EXPERIMENTAL

The devices fabricated at Hewlett-Packard (3) have the structure as shown in Fig. 1. Polysilicon of 0.5 μm thickness was formed by LPCVD on top of a 1000 Å thick layer of silicon

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nitride previously deposited on a single-crystal silicon wafer. After the polysilicon was implanted with boron (doses of 2×10^{11} or $3 \times 10^{11}/cm^2$ at 100 keV), it was laser-annealed at Stanford with a scanned cw argon laser (1). Subsequent processing at Hewlett-Packard followed a modified LOCOS (4) technology. The depletion-mode load transistors were formed by a selective implant through the gate oxide with phosphorous doses of 7×10^{11} and $1.4 \times 10^{12}/cm^2$ at 150 keV.

Devices of 2 geometries (large geometry with W = L = 20 μm, and small with W = 5 μm, L = 4 μm) were tested. While most of the tests were carried out in the above devices, functional devices of W = 4 μm, L = 3 μm have also been obtained. On a curve tracer these transistors appeared well behaved, with well-saturated, square-law characteristics seen on the large-geometry transistors at moderate drain voltages. At higher drain voltage the current began increasing with increasing drain voltage. This so-called "kink effect" has been observed in silicon-on-sapphire transistors (5). For the small geometry devices, short-channel effects similar to those seen on single crystal control wafers prevented the occurrence of a well-saturated region. The onset of the kink effect was still easily observed (Fig. 2).

Some source-drain leakage current was observed in the enhancement-mode devices which could be eliminated by applying a negative bias ($\sim$ -2V to -6V) to the single crystal substrate. Such a bias tends to accumulate the bottom surface of the polysilicon, which eliminates the effect of possible high fixed charges at the polysilicon/silicon-nitride interface, and the generation of current through generation centers in the polysilicon near the interface. Subsequent measurements were made with a substrate bias, unless otherwise noted.

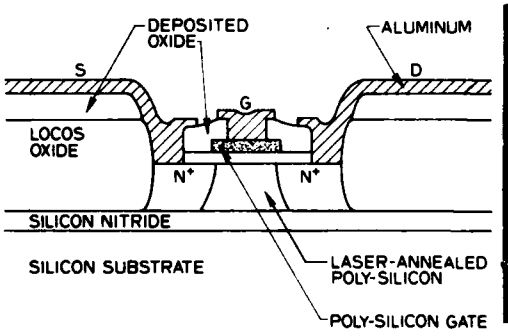

FIGURE 1. Schematic representation of transistor cross section.

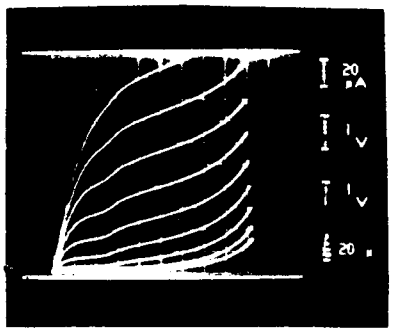

FIGURE 2. I-V characteristics of an enhancement mode device, with W=5μm, L=4μm, t_{ox} = 1060A, V_G = 0 to 8V.

The threshold voltages of the enhancement-mode devices (measured at 1 μA in the saturation region, V_D = 2.5V) were 1.4 V on the large-area devices and 1.1V on the small-geometry devices. The depletion-mode implant of 1.4 x $10^{12}/cm^2$ shifted the threshold voltage of the large-area transistors by -2.5V. There is a variation in the threshold voltage in both the enhancement-mode and depletion-mode transistors of about 1V.

The channel electron mobility was calculated from the large geometry transistors to be about 270 cm^2/V-sec, with variations generally in the range of 200-300 cm^2/V-sec. The depletion-mode transistors showed similar mobility values.

The source-drain leakage current at V_D = 5V with the gate biased below threshold was generally in the range of 1-10 pA/μm of gate width for the small geometry devices. Under a small value of V_D, lower leakage currents have been measured. At V_D = 0.1V, the small geometry devices indicated a leakage of 0.2 - 0.9 pA. Without a substrate bias, leakage current could be as high as 1 μA/μm of gate width.

A nine stage monolithic ring oscillator was fabricated. Each oscillator stage contained an enhancement-mode driver transistor with L = 4 μm and W = 9 μm and a depletion-mode load transistor with L = 8 μm and W = 4 μm. Oscillations were consistently observed with a supply voltage of approximately 14 - 16V. The period of oscillation averaged 70 nsec, giving a propagation delay of about 4 nsec per stage. The high operating voltage resulted from the nonoptimum thresholds of both the enhancement and depletion-mode transistors. A higher threshold voltage for the enhancement-mode transistor coupled with a lower zero bias current for the depletion-mode transistor would decrease the required supply voltage.

Replacement of the nitride layer in the above structure with a thick oxide layer would reduce the corresponding parasitic capacitance. Devices at Texas Instruments (6) were fabricated with 0.5 μm thick polysilicon deposited by LPCVD on 1 μm of SiO_2 grown on p-type <100> single-crystal silicon substrates having a resistivity of 6-8 Ω-cm. The wafers were then thermally annealed at 1100°C in flowing N_2 for one hour, which

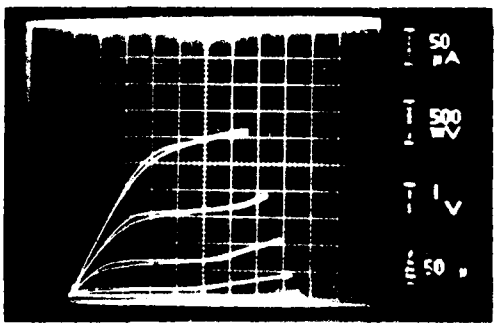

FIGURE 3. I-V characteristics of enhancement-mode device, with W=25 μm, L=5 μm, t_{ox}=400A, V_G=0 to 5V.

significantly improved the surface quality of the polysilicon films during subsequent laser anneal. They were then laser annealed at Stanford (1). The wafers were then processed to form N-channel MOSFETs using a previously established high-density (gate oxide = 35-40 nm) process. The patterning of the device islands was done by plasma etching in a manner similar for silicon-on-sapphire devices (7). Boron at an energy of 60 keV and a dose of 5 x $10^{11}/cm^{-2}$ was selectively implanted through the gate oxide to form enhancement devices, while depletion-mode devices were fabricated from the unimplanted regions. Transistors having W/L ratios of 25/5, 25/10, and 25/25 (μm/μm) were fabricated. The threshold voltages determined from measurements of $\sqrt{I_{DS}}$ against V_{DS} were 0.4V for the enhancement mode devices and -0.6V for the depletion mode devices. Surface mobilities were 170 and 215 cm^2/V-sec, respectively. An example of a 25/5 (μm/μm) enhancement mode device is shown in Fig. 3. In subsequent runs, devices of W = L = 40 μm, and W = 10 μm, L = 3 μm were fabricated. For the devices with W = L = 40 μm, surface mobility generally ranged from 350 - 400 cm^2/V-sec, and the leakage current at V_D = 5V with no substrate bias applied ranged from 1 - 10 pA/μm gate width. The devices with W = 10 μm, L = 3 μm showed more variation. The surface mobility ranged from 350 - 600 cm^2/V-sec. The leakage current at V_D = 5V with no substrate bias applied ranged from 1 μA - 1 pA/μm gate width, with typical leakage around 1 nA/μm gate width. A variation of threshold voltage of about 1V was also observed.

III. MINORITY CARRIER GENERATION LIFETIME MEASUREMENT

Different structures and fabrication procedures were used in the above devices. However, they showed no major differences in their performance. There is variation in individual device performance, particularly at small device dimensions.

The best devices performed comparably to the best devices in SOS. The low leakage current obtainable led us to investigate the minority carrier lifetime of the laser-annealed polysilicon (8). Transient capacitance measurements were made on MOS capacitors with the structure in Fig. 4. The polysilicon was 0.5 μm thick and was implanted with boron at a

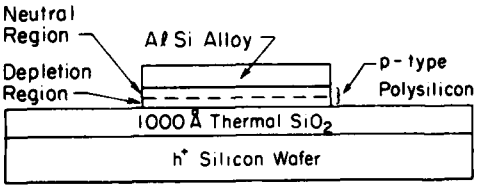

FIGURE 4 Schematic of MOS capacitor.

dose of 1 x $10^{12}/cm^2$ at 100 keV before annealing. The n^+ silicon wafer served as the gate to the laser-annealed polysilicon. From the time constant of the response (Fig. 5),

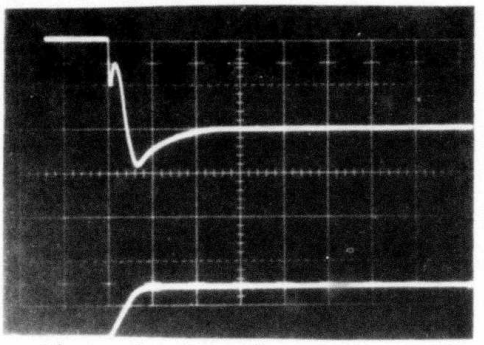

Figure 5. Transient response of MOS capacitor upper trace: capacitance 40 pf/div; lower trace: V_G 10V/div; zero of both traces: bottom line of scale; horizontal: 1 msec/div.

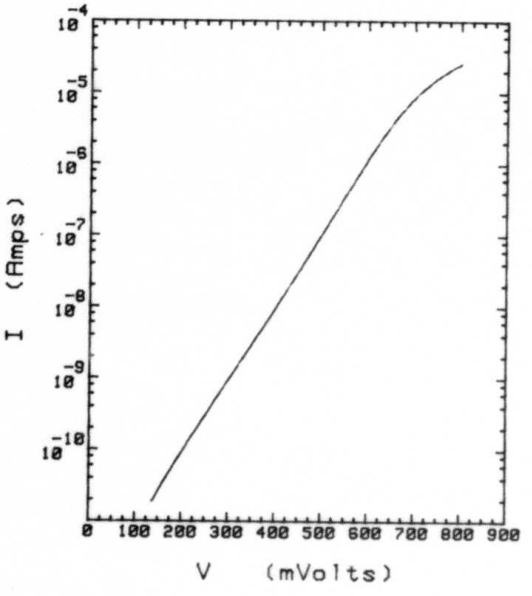

FIGURE 6. Forward I-V characteristics of diode.

a minority carrier generation lifetime of 0.4×10^{-9} sec was calculated (9). In the above calculation surface effects have not been included. The minority carrier generation lifetime was also estimated from a n^+p planar diode. The structure of the diode was similar to that of an enhancement mode MOSFET, except that one of the source and drain regions remained the same doping as the bulk (where boron was implanted at a dose of $1 \times 10^{13}/cm^2$ at an energy of 100 keV before laser annealing). The forward I-V characteristic of such a diode, with a width of 100 μm and a length of 75 μm, is shown in Fig. 6. Up to 600 mV, the slope was about q/1.6 kT, above which voltage series resistance in the diode became dominant. By an extrapolation of the current to around zero bias, where the recombination-generation current in the depletion region became dominant, the minority carrier generation lifetime was calculated to be about 5×10^{-9} sec, as compared to about 10^{-11} sec obtained from diodes fabricated in conventionally prepared polysilicon (10). Such a calculation also did not include surface components, and also depended on extrapolation of the I-V curve. Hence it can only be regarded as an approximate estimate to the bulk minority carrier generation lifetime. However, the values obtained from the capacitor and the diode measurement are in fair order-of-magnitude agreement.

V. CONCLUSION

Enhancement-mode and depletion-mode MOSFETs have been fabricated in laser-annealed polysilicon films using procedures compatible with current MOS technology. Such devices show performances comparable to those achieved in single crystal silicon or silicon-on-sapphire. A ring oscillator has been fabricated showing the possibility of integrated circuits in laser-annealed polysilicon. Leakage current of the transistors match the best reported values for SOS. Minority carrier generation lifetime measurements indicate a value comparable to, or better than, that obtained in SOS.

IV. ACKNOWLEDGMENTS

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Laser and Electron-Beam Solid Interactions
and Materials Processing

CW LASER-RECRYSTALLIZED POLYSILICON AS A DEVICE-WORTHY MATERIAL

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ABSTRACT

The basic crystallographic and electronic properties of cw laser recrystallized thin polysilicon films are presented and shown to be suitable for fabrication of MOSFET devices. Devices and simple integrated circuits fabricated to explore the potential of this material have electrical characteristics similar to devices fabricated on single crystal material and offer significant promise for future applications.

INTRODUCTION

Heavily doped polycrystalline silicon (polysilicon) is a material that is widely used in present day silicon integrated circuit technology for gates and interconnection lines in MOS integrated circuits. Initial interest in the beam annealing of polysilicon arose because of its potential as a process that could be used to promote grain growth and hence obtain resistivity reduction in these thin, heavily-doped films. Experiments undertaken to explore that potential [1] show that substantial reductions in resistivity can indeed be obtained and further that the electronic properties of cw beam-recrystallized, heavily doped polysilicon films closely approximate those of single crystal material. This latter result led us to what proved to be successful attempts to fabricate MOS transistors and integrated circuits directly in beam recrystallized polysilicon [2-4]. A substantial interest now exists in the potential of beam recrystallized silicon-on-insulators (SOI) as a substrate for integrated circuit fabrication. The purpose of this paper is to review the present state of this field.

Our development of this subject will begin with a discussion of the mechanism by which thin films of polycrystalline Si are recrystallized by a scanning cw beam. In Section 2 we discuss carrier velocity-vs-electric field measurements made on laser recrystallized films. We then describe the oxidation kinetics and interface properties of oxides grown on recrystallized polysilicon films, leading to a discussion of the electrical characteristics of MOSFETs fabricated directly on this material.

1. BEAM RECRYSTALLIZATION OF THIN POLYCRYSTALLINE FILMS

We describe first the annealing of thin polysilicon films irradiated by a cw argon laser, with emphasis on the relation between laser power and the surface morphology, dopant distribution and crystal structure of the annealed films.

Sample Preparation. The polysilicon films used for these studies were 0.57μm thick layers deposited by low pressure chemical vapor deposition (LPCVD) on a 1000 Å thick layer of either thermally grown SiO_2 or CVD Si_3N_4 on a Si substrate. In most cases the depositions were performed in commercial LPCVD reactors currently used for integrated circuit fabrication. After deposition, the wafers were doped by either ion implantation or thermal diffusion and then subjected to the beam processing operations.

Beam processing was performed in the scanning apparatus described in [5]. For laser processing, a cw argon laser was operated in the multiline mode with

a laser beam width on the sample surface of ~40 μm. This spot was scanned across the surface at a rate of 12.5 cm/sec in all cases to be discussed. The variables employed were substrate temperature, laser power, and the amount of overlap between adjacent scan lines. It is advantageous to use substantial substrate thermal bias (350°C) so that relatively small in laser power will produce substantial surface temperature of the irradiated film. For the experiments reported below, laser power was increased in 1 W increments from 5 W to 13 W, corresponding to a range of surface temperatures from ~600°C to 1500°C.

It should be emphasized that, while these conditions can produce very desirable changes in the properties of the film, they are certainly not the only set of conditions that would achieve these results; a different laser spot size, scan rate, laser power and substrate temperature can be chosen to yield very similar results.

Growth Mechanism. To study the mechanism of crystallite growth, arsenic ions were implanted into separate samples to serve both as a dopant and a marker which could be used to investigate the recrystallization process. The results of laser processing on surface morphology were studied by Nomarski interference contrast microscopy. For samples annealed at low and medium laser power levels (5 and 9 W respectively), no significant change in surface morphology was observed. Above 10 W, however, distinct lines were apparent in the nonoverlapped sample with the microstructure inside the line pointing in the direction of the scan. Figure 1 is a SEM micrograph of an annealed line obtained in this high power region, showing the directionality in the line, the smoothing of the original finely-textured surface, and the formation of large surface structures.

Fig. 1. Summary of the effects of laser power on the annealing of polysilicon and the corresponding measurement methods.

A qualitative description of the recrystallization process can be developed from a consideration of surface temperatures obtained during recrystallization. For the experimental parameters listed above, the surface of the film first reaches its melting temperature at a power per unit radius of ~1000 W/cm, which occurs at a laser power of ~5 W. However, when the surface melts, the reflection coefficient R changes from ~0.4 to ~0.6, thus reducing the power absorbed by the film. Increasing the power level above 5 W will therefore increase the thickness of the melted layer only slowly, until a power level of 10 W is reached, at which point the power absorbed in the film is still sufficient to produce surface melting even for the increased value of R corresponding to the molten surface. Melting may then proceed rapidly throughout the film.

Dopant Distribution. [6] Secondary ion-mass spectrometry (SIMS) was used to obtain dopant-profile measurements corresponding to the various power levels described in the previous section. Oxygen primary ion-bomardment and positive secondary ion-mass spectrometry were employed, using the CAMECA IMS-3f ion microanalyzer. Sensitive measurements of the As profiles required secondary ion initial kinetic discrimination to reduce the amount of $(^{30}Si^{29}Si^{16}O)^+$ detected at the same nominal mass as $^{75}As^+$. This analysis was sufficient to provide an As detection limit of 3-5 x 10^{18} atoms/cm^3. As can be seen

in Fig. 2, the high oxygen content of SiO_2 and minor surface-charging effects produce an anomolously high mass-75 intensity that misrepresents the true arsenic content in the oxide region. This problem, however, did not hinder the measurements in the polysilicon layer.

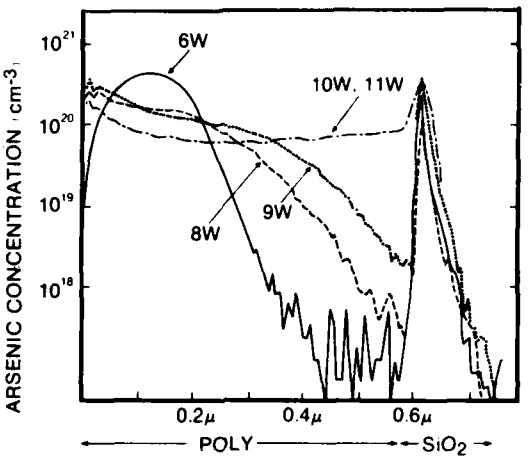

Fig. 2. Impurity redistribution in laser recrystallized polysilicon films.

As can be seen in Fig. 2, the dopants did not move from their as-implanted positions when the laser power was 6 W. The profile is approximately Gaussian and can be adequately predicted from Lindhard-Scharff-Schiott (LSS) range calculations [7]. Increased laser power results in deeper impurity penetration into the polysilicon.

When the power level was raised to 11 W, the dopant profiles became flat throughout the polysilicon layer. From TEM micrographs measured at 9 and 11 W it can be seen that, although partial melting occurred at 9 W, the grains are still small (~ 0.3 μm). Their growth is considerable (~ 20 μm) only when the melt front reaches the underlying oxide layer.

Crystal Orientation of the Beam Recrystallized Films [8]. In this section we describe the structural changes produced by cw laser recrystallization as they are measured by X-ray diffraction. Data will be presented for polysilicon films deposited on both silicon dioxide and silicon nitride since these are the most common films employed in present technology.

For these experiments films of low pressure CVD polysilicon were deposited at 625°C to a thickness of ~ 5500 Å. Some samples of each type were thermally annealed at 1100°C employing nitrogen since this heat treatment has been found to ease control of the laser recrystallization process. The samples were laser laser processed with the cw scanning argon laser under the melting conditions just described so as to form large grain structures.

A conventional X-ray diffractometer was used to analyze the samples. Measurements were taken with the samples mounted both parallel and perpendicular to the laser scan direction, but no anisotropy was seen. The results reported in Table 1 are the average of the two measurements. The intensities of the signals from the (111)-, (220)-, (311)-, (400)-, and (331) peaks were measured and normalized to indicate the relative amounts of crystallites with (111)-, (110)-, (311)-, (100)-, and (331)orientation in each film. The measured signals were normalized to account for the signal strengths expected in a thick, randomly oriented sample, and also for the finite film thickness.

The normalized X-ray results show that the (110) orientation is dominant in all the films immediately after deposition, with the normalized intensity being about ten times larger than that from any other orientation. Thermal annealing of the samples at 1100°C decreases the preference for (110) texture, although this orientation is still dominant. After laser recrystallization the (111), (311), and (311) orientations all increase significantly, with little difference seen between the films deposited on silicon nitride and those deposited on silicon dioxide. The influence of this mixed orientation on the oxidation rate and interface charges of structures containing laser-recrystallized polysilicon will be discussed below.

2. VELOCITY-FIELD CHARACTERISTICS

To assess the potential of these films for MOSFET applications, it is useful to know at least empirically how grain boundary scattering will affect the carrier velocity-vs-electric field characteristics, especially in the high electric field region. Measurements of election velocity in both laser recrystallized and silicon-on-sapphire films made by Cook et al. [9] are shown in Fig. 3, where we also include for comparison measurements made on single crystal material by Norris and Gibbons [10]. As can be seen, the electron velocity in heavily doped, laser recrystallized polysilicon films is actually larger than that in SOS films, even though the SOS films are more lightly doped. Neither of the films gives the sharp saturation and high terminal velocity that are characteristic of single crystal material, though adequate velocity is obtained for device purposes.

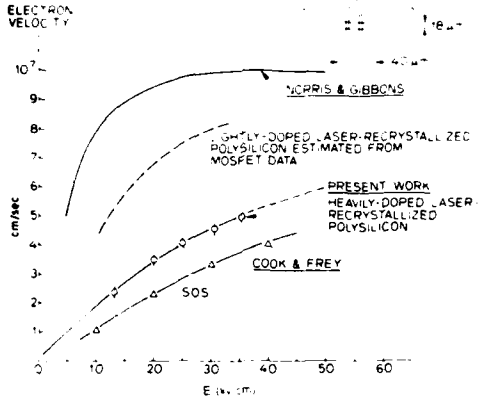

Fig. 3. Electron velocity vs. electric field in Si, SOS and laser-recrystallized polysilicon.

3. OXIDATION CHARACTERISTICS [8].

To complement the structural investigation, experiments were conducted to to determine the oxide thickness grown on laser-recrystallized polysilicon under conditions which might be used in an integrated-circuit process. For this investigation, only polysilicon films deposited onto silicon nitride with no subsequent nitrogen anneal were studied. After laser recrystallization, some of the wafers were doped by a 950°C, $POCl_3$ predeposition which produced a sheet resistance of 10 $\Omega/\square$ in single crystal silicon. Both undoped and doped films were then oxidized.

Two different oxidation cycles were used. A 125 min, 1000°C TCE/O_2 oxidation, which forms 1000 Å of oxide on (100)-oriented, single crystal silicon, was used in some cases. A 210 min, 800°C steam oxidation was also investigated to emphasize the effects of the silicon orientation and structure. The oxide thicknesses were measured on the polysilicon and single crystal control wafers with a UV spectrophotometer. After the oxide thicknesses were measured, the oxidation cycles were repeated without stripping the oxide so that thicker oxides, which could be measured more easily, were grown.

The oxide thicknesses after the first oxidation cycle are shown in Table 2. Analysis of these data lead to the conclusion that the oxide thickness grown on laser-recrystallized polysilicon is roughly the same as would be grown on the fastest-oxidizing direction of single crystal material under the same oxidation conditions.

TABLE I
Preferred orientation in laser-recrystallized polysilicon.

Sample	Insulating film	Thermal anneal	Laser processing	Laser power (W)	Grains	Normalized x-ray texture (111)	(110)	(311)	(100)	(331)
16-U	Si_3N_4	no	no	...	fine	25	720	78	0	~58
16-1	Si_3N_4	no	yes	8	long	335	133	363	~156	168
16-3	Si_3N_4	no	yes	10	long	445	183	342	~135	174
15-U	Si_3N_4	yes	no	...	fine	250	478	200	0	194
15-1	Si_3N_4	yes	yes	8	large	395	68	308	208	219
14-U	SiO_2	no	no	...	fine	50	615	62	0	~65
14-1	SiO_2	no	yes	8	long	365	379	262	198	245
13-U	SiO_2	yes	no	...	fine	258	491	150	~83	226
13-1	SiO_2	yes	yes	8	mixed	193	595	249	167	168
13-3	SiO_2	yes	yes	11	large	485	234	275	260	194

TABLE II
Oxide thickness on laser-recrystallized polysilicon

Doping	Oxidation temperature (°C)	Oxidizing ambient	Oxide thickness (Å) Polysilicon Recrystallized	Fine-grain	(100)	Single-crystal silicon (111)	(110)
undoped	1000	TCE/O_2	1050	1060	980	1100	~1120
undoped	800	steam	1930	1830	1140	1670	~1770
phosphorus doped	800	steam	6190	4830	6030	6000	

4. INTERFACE STATES [10].

Device measurements made by Lee et al. [2-4] show that when the top surface of a laser recrystallized polysilicon film is oxidized, a Q_{ss} value in the range $1.2 \times 10^{11}/cm^2$ is obtained. To investigate the behavior of the lower insulator/polysilicon interface, capacitor structures were fabricated and capacitance-voltage measurements were made with the depletion region extending into either the film or the underlying substrate, depending on the doping conditions employed. Both thermally grown silicon dioxide and low pressure CVD silicon nitride were investigated as the insulating layer.

All of the structures studied in these experiments were fabricated on n-type silicon wafer substrates. A 1000 Å thick, TCE/O_2 gate oxide was grown on some substrates at 1000°C, while others were covered with 1000 Å of low pressure CVD silicon nitride. A 5500 Å-thick film of LPCVD polysilicon was then deposited

at 625°C on all wafers. The wafers which contained an oxide layer were next annealed at 1100°C in N_2 for 1 hour to ease control of the subsequent laser recrystallization process. Wafers containing a nitride layer did not require this thermal annealing step. All polysilicon films were then implanted with boron at 100 keV. Portions of each wafer were recrystallized with a scanning cw argon laser, as described previously. Aluminum was then deposited and defined into squares 300 or 900 μm on a side, the aluminum serving as a contact to the recrystallized polysilicon. The polysilicon was plasma etched using the metal as a mask to provide the final geometry. After a 450°C H_2 anneal, the high frequency (1 MHz) capacitance voltage characteristics were measured. By using a lightly doped film on a heavily doped substrate, depletion regions can be made to extend into the polysilicon so that the properties of the polysilicon/ insulator interface can be measured. By using a heavily doped polysilicon film and a lightly doped substrate the properties of the SiO_2/Si(XTAL) interface can be probed to measure changes resulting from melting the overlying polysilicon film.

(a) Recrystallized Films on SiO_2. The structures with silicon dioxide beneath the polysilicon will be considered first. Laser powers of 14-16 W produced overlapping scans and the desired large-grain structure in the polysilicon. In the laser-recrystallized areas well-defined accumulation and inversion regions are observed in the capacitance-voltage characteristics. The capacitance with the polysilicon surface accumulated corresponded to an oxide thickness very close to the 1000 Å target thickness. When the opposite polarity voltage was applied, the capacitance decreased to a value indicating a depletion region approximately 2000 Å wide in the polysilicon. This depletion width is consistent with the hypothesis that all the dopant is activated by the laser recrystallization.

After a negative bias-temperature stress to insure that any positive mobile ions present did not influence the results, the flatband voltage in the laser-recrystallized regions was found to be in the range -2.9 to -3.4 V. If V_{MS} is taken to be -0.90 V, the fixed-charge density is calculated to be about 4×10^{11} cm^{-2}, which is somewhat higher than that expected in single-crystal silicon but not unreasonable since the X-ray measurements described earlier indicate a crystal structure containing grains of various orientations (and therefore various values of Q_{ss}).

The voltage between the measured flatband and inversion points of the C-V characteristic was greater than calculated, however, suggesting the presence of some fast states or lateral nonuniformities. If this distortion in the curve were entirely related to fast states, their density between flatband and inversion would be about 2×10^{11} cm^{-2}.

Thus, the properties of the silicon dioxide/polysilicon interface under a layer of laser-recrystallized poly-silicon resemble, but are inferior to, those at the interface between a thermally grown oxide and single crystal silicon.

(b) Polysilicon Films on Si_3N_4. Capacitors containing an insulating layer of silicon nitride were also tested. In all cases, the maximum capacitance corresponded to a silicon nitride layer with a relative permittivity of 7.0 for the 1000 Å thickness deposited. However, no meaningful value of the fixed charge or fast-state density could be extracted from the capacitance voltage measurements because of apparent electron trapping in the insulator. Furthermore, even before a bias-temperature stress, the flatband voltage changes significantly when large voltage ramps are applied. These results show that the polysilicon/silicon nitride interface is not well behaved, a situation similar to that of a silicon nitride/single crystal silicon interface.

(c) Interface Properties at the SiO_2/Si(XTAL) Interface. Capacitance-voltage characteristics were also measured to determine the interface properties at the underlying SiO_2/Si(XTAL) interface. When a device-quality SiO_2 layer was grown as the insulator, this interface had an as-prepared value of $Q_{ss} \sim 5 \times 10^9/cm^2$. After laser processing of the polysilicon film to form long grain structures, Q_{ss} at the SiO_2/Si(XTAL) interface increased to 5×10^{10}-

$10^{11}/cm^2$, which is higher than the original value but still sufficiently small to permit device fabrication in the underlying Si.

5. CHARACTERISTICS OF MOS DEVICES AND INTEGRATED CIRCUITS FABRICATED ON LASER RECRYSTALLIZED POLYSILICON FILMS

The electronic properties of cw beam annealed polycrystalline films just described strongly suggest that these films can be used directly for the fabrication of active devices. A number of studies have been performed to evaluate this possibility. Most of these evaluations have been performed using MOS field effect transistor structures, since these devices utilize majority carrier properties and should be minimally sensitive to lifetime and grain boundary effects that could dominate the characteristics of bipolar devices. Channel lengths for MOS transistors that are on the order of, or smaller than, the grain size in the laser recrystallized films may be expected to yield device performance that is comparable to that of devices fabricated in single crystal silicon, whereas the properties of grain boundaries have been found to dominate device behavior when devices are fabricated on fine grain polysilicon films [11]. In what follows we discuss the electrical characteristics of MOSFETs fabricated on such films under a variety of different conditions.

MOSFETs Fabricated on Polysilicon/Si_3N_4 Substrates [2]. The first MOSFET devices made on laser recrystallized polysilicon films were reported by Lee et al. [2]. The processing steps utilized for both depletion and enhancement devices are described in that reference.

Devices with channel lengths of 10, 20, and 50 μm were fabricated; the channel widths were 250 μm for the depletion mode devices and 270 μm for the enhancement mode devices. Since the grains formed by laser annealing tend to align themselves with the laser scan directions, the channels were fabricated both parallel and perpendicular to the laser scan direction. No difference in drain characteristics was observed for these two orientations of the channel.

The source-drain I-V characteristics of both the enhancement and depletion mode devices are shown in Fig. 4. Since the current in a depletion mode transistor flows through the entire thickness of the conducting layer, film properties can be calculated from the transconductance and drain current. In the linear region the transconductance is as follows:

$$g_m = \frac{I_D}{V_G} = C_{ox} \frac{\mu W}{L} (V_D - V_S).$$

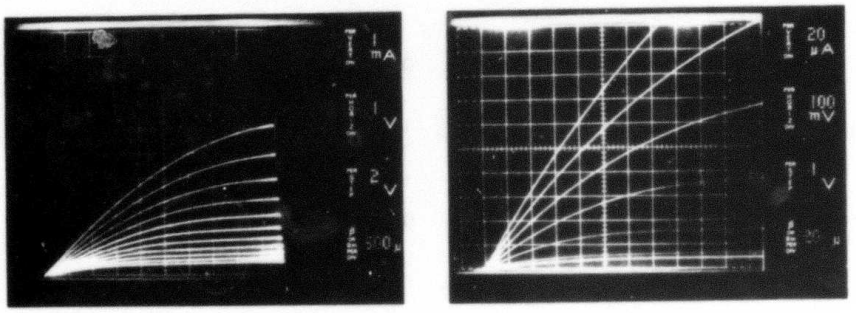

Fig. 4. (a) Source-drain I-V characteristics for a depletion-mode device (V_G = 0 to -12 V). (b) Source-drain I-V characteristics for an enhancement-mode device (V_G = 0 to 7 V).

From the transistor channel geometry (L = 50 μm, W = 250 μm), the mobility is calculated to be 450 cm^2/V-sec, compared to a mobility of 750 cm^2/V sec in single crystal silicon at a dopant concentration of 6 x 10^{16} cm^{-3}, which corresponds to the dose implanted into the polysilicon film.

For the enhancement mode device the field effect mobility was similarly calculated from the source drain characteristics in the linear region and the device geometry (L = 50 μm, W = 270 μm) to be 340 cm^2/V sec. This value may be compared to the value of 630 cm^2/V-sec expected for the field effect mobility in single crystal silicon of the same dopant concentration.

The threshold voltage (defined to be the gate voltage which induces a drain current of 1 μA) was measured to be +2.5 V. Again, assuming Q_{ss}/q = 2 x 10^{11} cm^{-2}, the threshold voltage is calculated to be -0.2 V in the absence of defect levels in the polysilicon. The difference between the measured and calculated threshold voltages may be attributed to the charging of defect levels before the surface can be inverted, as well as to uncertainties in the value of Q_{ss}/q used in the calculations.

Ring Oscillators on Polysilicon/Si_3N_4 Substrates. The gate lengths utilized in the MOSFETs described in the previous section were sufficiently large to cover many grain boundaries, and in addition the devices were not constructed in such a way as to permit basic speed of response measurements to be made. To study such characteristics, ring oscillators were fabricated using transistor geometry compatible with current high performance MOS I-C technology. Both enhancement and depletion mode transistors were fabricated using a production I-C process, and a functioning, integrated ring oscillator containing both enhancement mode driver transistors and depletion mode load elements was constructed. Details of the device construction process and the I-V characteristics of separate transistors are given in Ref. [4].

The monolithic ring oscillator consisted of nine nearly identical oscillator stages and three output buffer stages. Each oscillator stage contained an enhancement mode driver transistor with L = 4 μm and W = 9, 30, and 133 μm on successive stages, and similarly scaled depletion mode load transistors. Both devices of each stage were contained in one dielectrically isolated silicon island since the intermediate node is common to both transistors.

Oscillations were consistently observed with a supply voltage of approximately 14 - 16 V. The period of the output signal averaged 70 ns. Calculation of the capacitances from the device dimensions indicates that 60 percent of the 0.8 pF capacitance which must be charged to change the state of each stage is associated with the thin nitride under the polysilicon. Reducing this contribution by the use of a thick oxide or an insulating substrate would significantly reduce the overall capacitance, with a corresponding decrease of the propagation delay time.

MOSFETs and Ring Oscillators on Polysilicon/SiO_2 Substrates. The experiments described in the previous section show that MOS devices can be fabricated on the top surface of laser recrystallized films with electrical properties that are far superior to those obtained in as deposited material, and comparable to similar device characteristics obtained when single crystal silicon substrates are employed. However, as suggested earlier, the thin nitride layer employed makes electrical isolation from the substrate difficult, and is furthermore not an ideal choice as an insulating layer because of the surface states at the nitride-silicon interface. For integrated circuit applications, a thick oxide layer is a better choice as an insulating material. Hence both MOSFETs and ring oscillators have been fabricated on laser recrystallized films prepared on SiO_2 substrates. The fabrication details of these devices are discussed in Refs. [3,4].

(a) MOSFETs. Enhancement and depletion mode transistors having W/L ratios of 25/5, 25/10 and 25/25 (μm/μm) were fabricated on both laser annealed and unannealed areas of the wafers to provide a direct comparison of device type and annealed against unannealed polysilicon on the same wafer.

The threshold voltages for these devices, determined from measurements of I_{DS} against V_G, were 0.35 - 0.45 V for the enhancement devices, and -0.5 to -0.7 V for the depletion devices. In the unannealed areas of the wafer, the measured threshold voltages of the polysilicon transistors ranged from 7 to 10 V, with little if any difference between implanted and unimplanted devices. The mobilities were determined from the measured slope of the drain-source current (I_{DS}) against gate voltage (V_G) curves at low drain voltage (V_D = 0.1 V). The measured surface mobilities were 170 and 215 cm^2/V_{sec}, respectively, for the n-channel enhancement and depletion devices. These values compare favorably with 400-500 cm^2/V_{sec} and 600 - 650 cm^2/V_{sec} which are obtained in present n-channel SOS devices (using 0.5 μm silicon layers) and bulk NMOS devices, respectively. The measured surface mobilities on unrecrystallized polysilicon devices ranged from 23 - 29 cm^2/V_{sec}, which is in agreement with previous reported results.

The leakage current between the source and drain in the off condition was also examined, in view of the difficulty in achieving low leakage in SOS devices. With the gate and source grounded and 5 V on the drain, the measured source-drain leakage currents were 25, 50, and 160 pA for gate lengths of 25, 10 and 5 μm, respectively. All devices had channel widths of 25 μm. These results correspond to leakages of 1 - 6 pA per micrometer of channel width, and match the best reported values for SOS.

(b) Ring Oscillators [4b]. Ring oscillators have also been fabricated on laser recrystallized films deposited on thick oxide layers. The individual inverter stages in these ring oscillator circuits consisted of 6 μm channel enhancement mode driver devices with a deep depletion device as load. Each stage was constructed with a fan out of three, with a two stage source follower output on each ring oscillator as a buffer. Both seven and eleven stage ring oscillators were fabricated, both being functional and of very similar performance.

The delay per stage and the power delay product of an eleven stage ring oscillator were plotted as a function of the supply voltage (V_{DD}). These results were obtained for the ring oscillator operating in the large signal regime, namely, inverting between V_{DD} and ground. The minimum propagation delay obtainable was 44 nsec per stage at 10 volts V_{DD} and the minimum power delay product for sustaining oscillation was 4.1 pJ. At 5 volts V_{DD}, the propagation delay and the power delay product were 57.5 nsec and 7 pJ, respectively.

Isolated enhancement mode devices, which have the same geometry as the driver in the ring oscillator circuit, were also characterized. A surface electron mobility of about 300 cm^2/V-sec (compared to 640 cm^2/V-sec measured in devices fabricated in bulk silicon slices), a threshold voltage of about -2 V and a subthreshold leakage current of about 10 nA per micron channel width with -5 volts gate voltage and 5 volts supply voltage were measured. Isolated depletion mode devices having the same geometry as the load device in the ring oscillator exhibited a typical threshold voltage of -3.6 volts and a drain current of typically 196 μA at 5 volts supply and with the gate grounded. The subthreshold current decreased by about 3-1/2 decades per volt gate voltage. The shape of the subthreshold I-V characteristics and the fact that the leakage current did not scale with the channel width indicate that edge-related leakage current dominates, a result not surprising since no channel stop implant was used. As a reference, the propagation delay in similar ring oscillators fabricated in bulk silicon, with a depletion width of 3 μm between the n^+ region and the substrate (and thus the same n^+ to substrate capacitance compared to that provided by the 1 μm thick oxide layer), and operating in the large signal mode is typically 36 ns at 5 volt V_{DD}.

Improvements Obtained with LOCOS Technology. The devices described so far were fabricated on continuous polysilicon films that were recrystallized prior to any subsequent device fabrication steps. Devices can of course also be fabricated on polysilicon islands that are defined prior to laser recrystallization; the possibility of fabricating single crystal islands [12] makes this procedure especially attractive. However, surface tension effects often cause the

initially rectangular polysilicon islands to take on a rounded, "loaf-of-bread" appearance after laser processing, especially if too much laser power is employed. Lam et al. [13] have recently shown that LOCOS technology can be employed to extend the range of laser powers for acceptable surface morphology after recrystallization. At the same time they obtained improved surface channel mobilities.

The basic LOCOS process as applied to the present problem is described in Fig. 5. A layer of Si_3N_4 is first deposited on the polysilicon film and patterned to produce the structure shown in Fig. 5(b). Next the polysilicon film is plasma etched to a depth such that a subsequent oxidation cycle will convert the remaining polysilicon completely to SiO_2 and at the same time return the oxidized surface to the original polysilicon surface. Lateral oxidation underneath the Si_3N_4 will produce the "birds beak" shown in Fig. 5(c). This process then yields dielectrically isolated polysilicon islands in which the edges are clamped by the surrounding SiO_2. Laser recrystallization and device fabrication are then carried out as before.

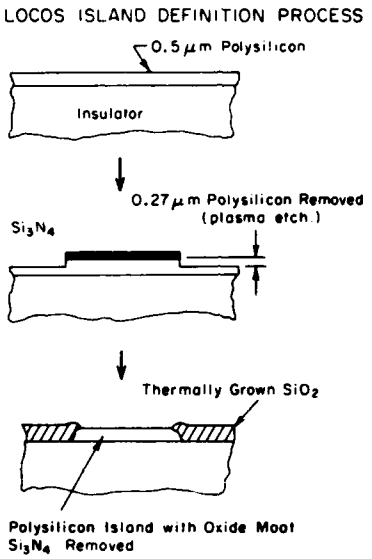

Fig. 5. LOCOS process for defining oxide-clamped polysilicon islands.

Devices fabricated on these films have surface mobilities that are generally superior to those obtained from laser recrystallized continuous polysilicon films. The basic results are summarized in Table 3, where it can be seen that surface channel mobilities comparable to the best obtained on single crystal silicon can be achieved.

One-Gate-Wide CMOS Inverters on Laser Recrystallized Polysilicon [14]. The experiments described in the previous subsections show that MOSFETs and ring oscillators can be fabricated on the free surface of a laser recrystallized polysilicon film to obtain devices with characteristics very similar to those that would be obtained with single crystal silicon. The interface charge measurements discussed in Section 4 also indicate that Q_{SS} values at both the crystalline silicon/SiO_2 interface and the SiO_2/laser recrystallized polysilicon interface can be kept at or below the mid-$10^{11}/cm^2$ level. These results suggest that devices can be made in which the bulk silicon is used for one device and the

TABLE III
Gate defect density and surface electron mobility for MOSFETs on oxide-clamped laser annealed polysilicon islands

Substrate Material	Laser Power (W)	# of Device Measured	% With Gate Defect	Number of Devices that Exhibit Surface Electron Mobility in the Range of (cm²/V-S)				
				>600	500 to 600	400 to 500	300 to 400	200 to 300
Oxide	6	20	45	3	5	2	1	
	5.5	49	43	7	13	6	2	
	5	58	24	5	11	14	10	4
	4.5	22	23		4	8	4	1
	4	33	42					1

bottom of the laser recrystallized polysilicon film is used for a second device. One structure that would benefit directly from this possibility is a one-gate-wide CMOS inverter in which the bulk silicon is used for the p channel device and the laser recrystallized polysilicon film for its n channel complement.

The basic device structure is shown in Fig. 6. The joint use of a single gate to drive both the n- and p-channel devices led Kleitman [15] to suggest the term JMOS to describe this structure.

To obtain the highest surface mobility for the particle with the lower bulk mobility, it is preferable to build the p-channel device in the single crystal substrate. Accordingly, fabrication was performed on an n-type <100> single crystal of Si of resistivity 1 - 4 Ω-cm. The fabrication sequence is described by Gibbons and Lee, Ref. [14].

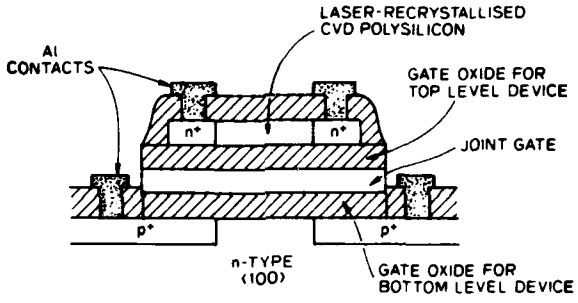

Fig. 6. Geometry of one-gate-wide CMOS inverter.

The drain characteristics of devices obtained by these authors show, for the p-channel device, which was made on the single crystal silicon, a threshold voltage of -2.2 volts and a surface mobility for holes of 180 cm^2/V-sec. These values are consistent with a Q_{SS} value of approximately 1.6×10^{11}. Threshold shifting could be performed using conventional implantation techniques and thermal annealing prior to fabrication of the gate as outlined above. For the n-channel device, a threshold voltage of 2.1 volts and a surface mobility for electrons in the laser recrystallized film of 160 cm^2/V_{sec} were obtained. These values are somewhat lower than those obtained in previous experiments but nonetheless sufficient to indicate that well-matched CMOS devices can be made in the two level ("high-rise") configuration envisaged as JMOS.

Polysilicon on Quartz. As a final example we discuss briefly the recent work of Kamins and Pianetta, [16] who have successfully fabricated MOSFETS on polysilicon islands that were deposited directly on quartz substrates. This process is of interest since it may permit the fabrication of image sensing devices and integrated circuits on potentially low cost substrates.

The main differences between these experiments and those discussed earlier arise from the different thermal conductivity and thermal expansion coefficient of the quartz substrate compared to a single crystal silicon substrate. The difference in thermal expansion normally causes substantial cracking of the polysilicon films upon laser recrystallization, leading to unstable film characteristics and surface morphologies. To circumvent this problem, stress relief grooves were etched through the polysilicon films to form polysilicon islands that could then be recrystallized successfully. A form of LOCOS technology was also employed, as suggested in Fig. 7, without first etching the polysilicon film to produce a uniform surface height after the oxidation cycle. The geometry employed to assess the device potential of these films is shown in Fig. 7(c). Devices fabricated to date on these islands have I-V characteristics that are similar to those fabricated on Si_3N_4 substrates, though little has been done as yet to optimize the processing parameters. It is possible that optimization studies could lead to a very useful technology for a number of important applications.

6. USE OF ARC SOURCES FOR RECRYSTALLIZATION OF POLYSILICON FILMS ON QUARTZ

One interesting feature of the recrystallization process on quartz substrates is that, since the substrate thermal conductivity of quartz is much lower than that of silicon, much lower beam power is required for long grain recrystallization. This idea has been exploited recently by Gibbons et al. [17], who use a

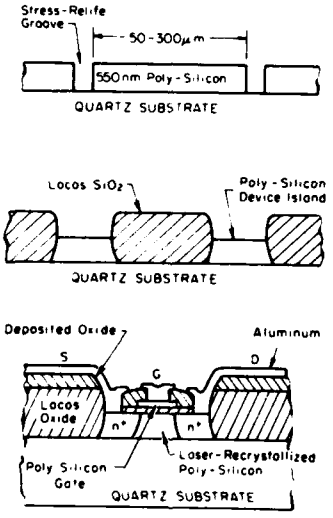

Fig. 7. Cross-sections of experimental device structures. (a) Stress-relief grooves etched into polysilicon film on quartz before laser recrystallization. (b) Silicon film defined into device islands by LOCOS oxidation before laser recrystallization. (c) Completed transistor structure.

cw xenon arc source to recrystallize continuous polysilicon films deposited on quartz. The system used for these studies is indicated schematically in Fig. 8; it consists of a stationary source focussed to a 1mm spot, and a heated, mechanically scanned sample holder.

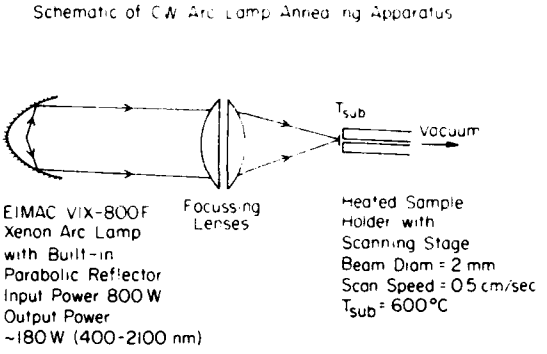

Fig. 8. Schematic of CW arc lamp annealing apparatus.

A Nomarsky micrograph of an arc-source recrystallized film is shown in Fig. 9 as an existence proof. The surface topology is clearly unacceptable for device fabrication. However, the use of stress relief grooves such as those employed by Kamins and Pianetta [16] and the development of optics that will produce a ribbon beam will most probably produce acceptable recrystallization at a substantially lower cost than can be obtained with laser-based recrystallization.

Fig. 9. Nomarsky micrograph of polysilicon film recrystallized by cw xenon arc source.

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